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Nanosensing with Si based nanowires

Deliverable D1.1: Pros and cons of nanowire fabrication techniques for sensor arrays

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Deliverable summary

Pros and cons of fabrication techniques for silicon nanowires (SiNW) is reviewed with respect to a multifunctional sensor application based on silicon nanowires integrated with CMOS. Bottom-up approaches is generally simple and can provide high quality SiNW with nanometer dimensions. We have drastically improved the morphology and composition control in the growth of SiGe NWs using bottom-up approach. However complex integration with CMOS and lack of ability to position many SiNW in an ordered way is still a challenge for bottom-up approaches. This last point could be solved by using an assembly of nanowires. Top-down approaches has less severe integration issues with CMOS technology. Electron beam lithography (EBL) has been used to pattern SiNW for sensors but throughput is still an issue for an application with many nanowires. In recent year advanced optical lithography and sidewall transfer lithography (STL) has evolved and has been shown to produce SiNW in the 10-50 nm range with high reproducibility and throughput. Within Nanofunction SiNW fabrication processes that are compatible with CMOS technology using EBL, advanced optical lithography and STL has been developed.

1. Introduction

Silicon nanowires (SiNW) have been shown to be an excellent sensing element to detect charged molecules due to the large surface to volume ratio. The sensitivity of an individual SiNW has shown to outperform planar structures such as nanoribbons for the same response time [1]. Furthermore it was found that reducing the dimension of the sensing element to Si dots does not substantially improve the sensitivity. Sensing applications includes detection of molecules in gases and in liquids and for several applications it is desirable to sense several different molecules with one sensor. This can be achieved by placing SiNW in a matrix and integrate them with CMOS for reading the state of an individual SiNW. To achieve the substantial potential of SiNWs in the area of a multifunctional sensor it will be required to achieve controlled and predictable assembly of well-ordered SiNWs. In this deliverable we report on the different SiNW fabrication processes and their applicability for a SiNW matrix sensor integrated with CMOS.

2. Fabrication techniques

The fabrication process of SiNWs can be divided into “bottom-up” and “top-down” approaches. We review the fabrication technologies for SiNW and describe pros and cons for a SiNW matrix sensor. We report the state-of-the-art and work performed during the first year within Nanofunction.

2.1 Bottom-up fabrication

Bottom-up nano-fabrication is in principle simple and provides many high quality materials. Silicon whiskers grown from the well-known vapour-liquid-solid (VLS) reaction have been extensively investigated [2-8]. In the VLS reaction, metal particles, for example gold particles on Si substrate, are generally used as the mediating solvent to direct the growth of SiNWs. Up to date, many other methods such as oxygen-assisted-growth (OAG) [9], [10], vapor-solid-solid (VSS) [11], electroless etching methods and laser-assisted catalytic growth (LAC) [12-14], have been developed to synthesize large-scale SiNWs.

In Nanofunction we have developed a generic process (same temperature and total pressure) to grow Si, Ge and SiGe NWs with Au as a catalyst based on the addition of HCl in the gas phase [15]. We found that diameter uniformity, growth stability and morphological quality are also drastically improved. The SiGe NWs were grown in a hot-wall reduced pressure chemical vapour deposition system via the VLS process on Si (111) substrates. Si and Ge are provided by pure silane (SiH4) and germane (GeH4 5% in H2). We have studied the growth of SiGe NWs as a function of 1) gas phase composition, 2) gas ratio: $R=\Phi_{GeH4}/(\Phi_{SiH4}+\Phi_{GeH4})$ where Φ_X is the flow of the precursor x expressed in sccm, and 3) growth temperature. Growth temperature and gas ratio have been fixed at 400°C and R=0.15 respectively. Fig. 1 shows SiGe NWs obtained with HCl flows varying between 0 and 90 sccm. Without HCl most of the NWs are highly kinked and the few straight NWs are slightly tapered. Moreover, an uncatalyzed growth of nanocrystals on the substrate can be observed. When 40 sccm of HCl is introduced along with process gases, the NWs are straights, and no tapering or uncatalyzed deposition on the substrate can be observed by SEM. TEM image show that the NW are single crystalline and grow along the (111) direction.

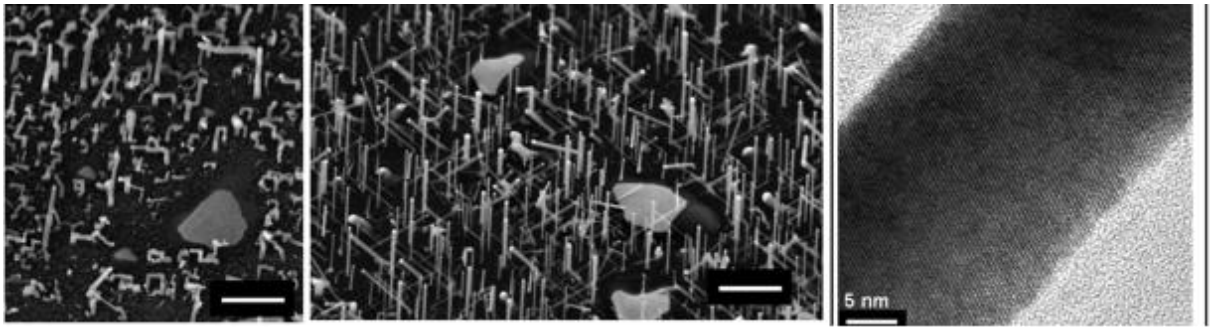

Fig. 1 SEM pictures of SiGe NW grown at 400 °C with R=0.15. Left image is without HCl and middle is with 40 sccm HCl. Right shows a HRTEM image of a single SiGe NW.

The gas flow ratio R was changed by keeping the germane flow constant (4.5 sccm of pure GeH4) and by varying the SiH_4 flow between 90 and 25 sccm (R varies between 0.048 and 0.15). Fig. 2 shows that the Ge fraction without using HCl evolves linearly between 20.9 and 38.4 % as R is changed from R=0.048 to R=0.09 (dark triangles). Then the Ge fraction tends to reach a saturation value around 50%. When we added 40 sccm HCl (white triangles), no saturation of the Ge fraction was observed.

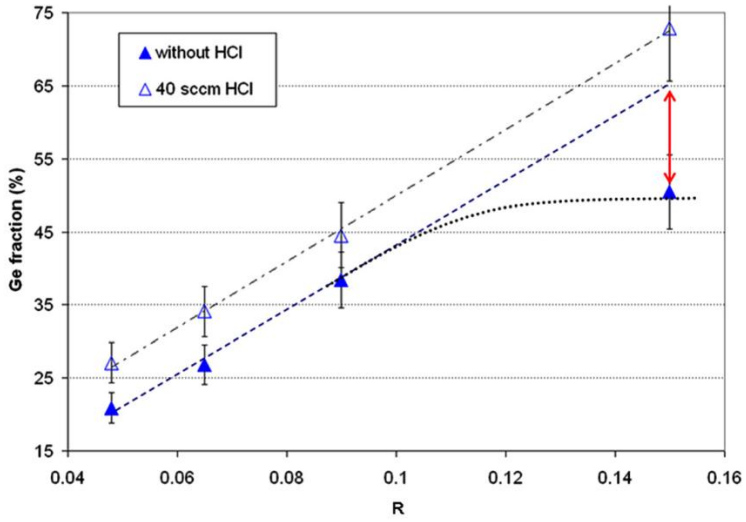

Fig. 2 Ge fraction of the SiGe NWs grown at 400 °C as a function of the GeH_4 gas flow ratio R. Without HCl, the Ge fraction for R=0.15 does not follow (red arrow) the linear tendency high-lighted for low R (dashed line). At 40 sccm flow of HCl, the Ge fraction seems to follow a linear increase (dashed-dot line) as a function of R

The HCl effect on Ge fraction was found to be temperature dependent. At 400°C and 425°C, an increase of the Ge fraction from 50% to 70% is observed when using 40 sccm HCl. At 450°C, two HCl flow rates have been used. At 40 sccm HCl induces an increase from 50% to 65% of the Ge content and at 90 sccm HCl leads to an increase of the Ge content from 50 to 85%. These results clearly show a remarkable effect of HCl addition in the gas phase on the Ge fraction in the NWs, which depends both on the growth temperature and on the flow rate of HCl. HCl improves the NWs' morphology and density of straight NW at reduced flow rates ($\Phi_{HCl} \leq 40$ sccm) and deteriorates or inhibits the growth at higher flow rates ($\Phi_{HCl} \geq 60$ scmm). HCl also

improves the incorporation of Ge atoms in the SiGe NWs and allows the growth of Ge rich SiGe NWs under conditions where Ge fraction would saturate at lower values without HCl. The SiGe NWs growth rate is decreased as HCl is introduced in the gas phase. Finally, HCl effects turn out to be temperature dependent and allow extending the process window toward higher growth temperatures. By adjusting HCl flow and temperature we are able to control precisely the morphology and the composition of the NWs for a broad range of growth temperature.

A potential drawback using gold and copper as catalyst to direct the growth of SiNWs by VLS or VSS techniques is the possibility of inducing defect levels in SiNWs, which would trap electrons and holes in Si, and then depress the optical and electronic properties of the nanowires. The bottom-up approach which is based on self-assembled chemical vapor deposition growth techniques has some limitations, such as complex integration, requiring transfer to substrates, difficulties in positioning an individual nano- structure, making reliable ohmic contacts and making it demanding to construct functional device arrays [16-28]. Nevertheless within Nanofunction high performance silicon nanowire filed-effect transistors with silicided contacts has been demonstrated (see Fig. 3) [29].

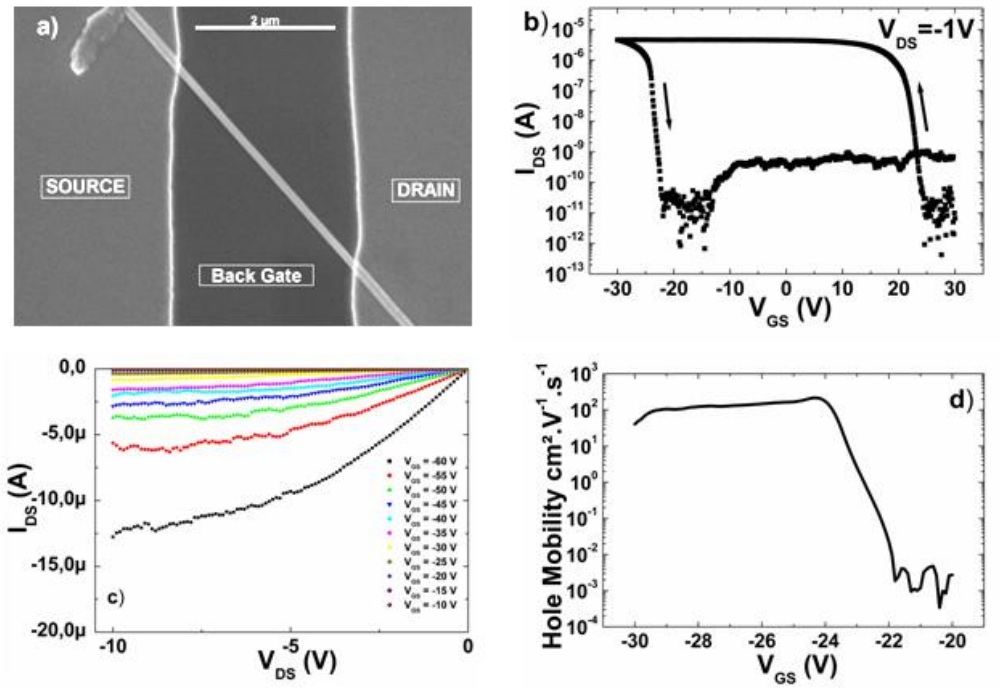

Fig. 3 SiNWs FETs with 200 nm Si3N4 back gate insulator: (a) A SEM view of the device showing S/D electrodes and a single SiNW bridging both contacts. (b) I_{DS}-V_{GS} characteristic of a SiNW FET recorded at V_{DS} =- 1 V. The on-off current ratio of this device is $2 \cdot 10^5$. (c) typical I_{DS}-V_{DS} characteristic of the devices. A saturation region is observed for high drain voltages inferior to -5 V. Measures were performed with a negative to positive gate voltage sweep which explains that the OFF-state occurs for negative gate voltages. d) Hole mobility reported as a function of the gate voltage at VDS = -1 V showing a maximum of 200 cm^2/Vs estimated from the transconductance of the device. The I_{DS}-V_{GS} in (b) was smoothed before the transconductance dIDS/dVGS was calculated.

The control of doping concentrations in self-assembled semiconducting nanostructures remains a challenge, and the fabrication of high-density sensor arrays is also very difficult. So far gold has dominated as the catalyst for growing Si nanowires via the vapour–liquid–solid (VLS) mechanism. Unfortunately, gold traps electrons and holes in Si and poses a serious contamination problem for Si complementary metal oxide semiconductor (CMOS) processing. To overcome this limitation, potential solutions exist and CMOS compatible catalysts based on silicides for Si NWs growth could be envisioned for SiGe NWs growth [30].

In an effort to address the problem of accurately position a huge amount of SiNW grown by “bottom-up” techniques hybrid approaches has been developed [31-35]. The grown-in-place approach is a kind of hybrid approach, in which electron beam lithography (EBL) as well as optical lithography are used to define catalyst metal in prospect channel and VLS growth is used to fabricate SiNWs guided by the catalyst.

Wafer- or chip-scale bonding and epitaxial growth represent the two most widely used methods for achieving these types of integrated systems. Nanowires were grown by chemical vapor deposition. The next step involves transferring these processed elements, with the use of an elastomeric stamp–based printing technique, from the source substrates to a device substrate.

The overall process involves (i) optimized growth of designed NWs by nano-cluster directed growth and (ii) patterned transfer of NWs directly from a NW growth substrate to a second device substrate via contact printing Devices and circuits are then fabricated on the printed arrays of NWs using conventional top-down lithography and metallization processes [32].

The hybrid approach extends the manipulation for nanostructures, and it becomes one of the major techniques for making SiNWs-related nano devices presently. These new assembly-based approaches overcome processing limitations of conventional planar CMOS technology and thus could make them formidable methods for the future high-performance 3D integrated circuits.

2.2 Top-down fabrication

Top-down nanopatterning techniques provide a different path for fabricating high-density, high-quality nanoscale sensors that can be integrated with Si-based signal processing and communication circuits. Several key advantages favoring top-down Si-NW nanofabrication include well established techniques for nanopatterning, semiconductor doping, electrical contact formation, and, very importantly, the commercial availability of high quality silicon-on-insulator (SOI) substrates [36-56].

Arrays of SiNWs with 15 nm lateral dimensions have been realized with nanoimprint lithography [37]. This is a relatively low cost technology that allows high resolution patterning, but the throughput is rather low. In addition, the replication stamp fabrication is complicated and can be costly depending on the life expectancy of the stamp. Furthermore patterning on wafer scale remains problematic.

Conventional top-down nanopatterning techniques, such as deep-UV and immersion deep-UV photolithography are currently the standard for semiconductor manufacturing. However, these techniques are extremely expensive and demand a high volume application in order to be cost-effective. Generally they are only accessible to large-scale integrated circuit manufacturers. Within Nanofunction advanced optical lithography (LETI) is used to directly pattern SiNWs with

dimensions down to 35 nm in width and length. Combined with electron beam lithography SiNW with lengths and widths down to 3 nm is fabricated. The main fabrication steps are depicted in Fig. 4. The choice has been to develop CMOS compatible fabrication steps in order to be able to integrate the sensors with its addressing and readout circuits. By doing so, the way toward a possible industrialization is considerably eased. 200 mm wafer are being used with industrial processing tools. The wafers with SiNWs will be cut into chips (see Fig. 4 for layout) to be able to provide samples.

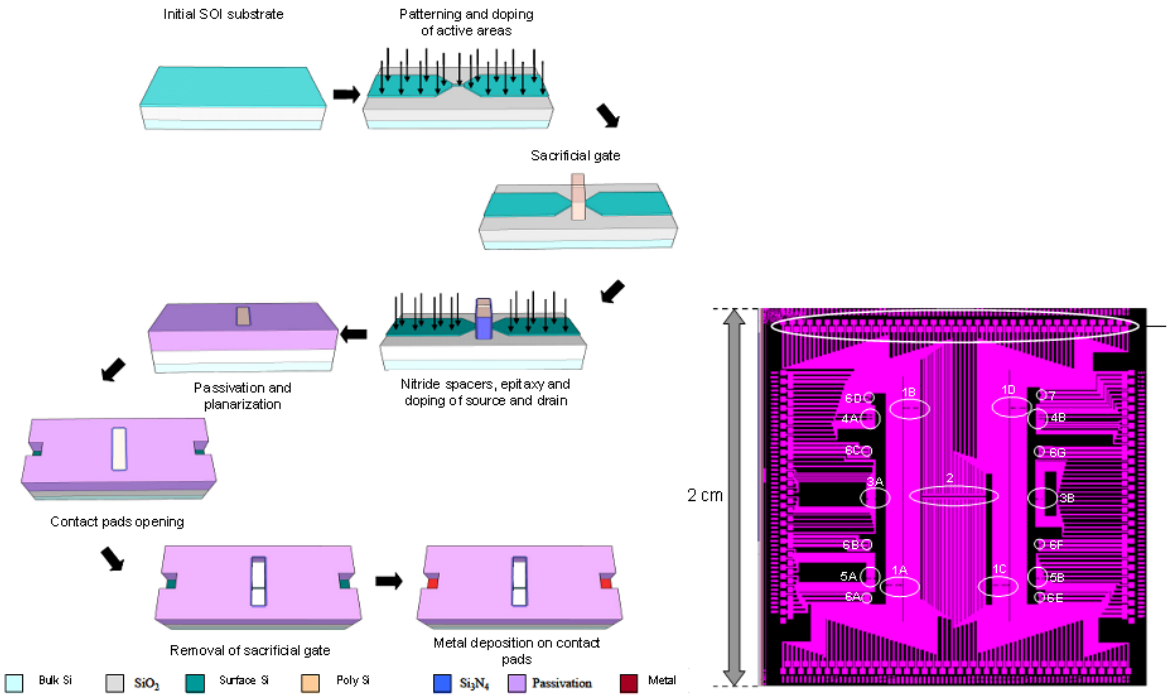

Fig. 4 CMOS compatible fabrication steps (left) to realize SiNWs with sub 10 nm dimensions as sensing element. The Layout of SiNW chip is depicted to the right (Nanofunction partner LETI).

For low volume applications G and I-line optical stepper lithography can be cost effective. However, these top-down patterning techniques can not directly pattern sub 100 nm features. Using Sidewall Transfer Lithography (STL) it is possible to pattern sub-30 nm wide SiNW with the high throughput achieved with stepper lithography [57], [58]. STL is a patterning technique in which lines are patterned by a combination of optical lithography and a spacer patterning process. A support material is patterned by optical lithography and etched anisotropic. A spacer is created on the sidewalls of the support material by conformal deposition and anisotropic etching. The support material is then removed by an etch leaving the spacer as mask for sub-sequential etching. Within Nanofunction (KTH) a STL process have been developed with the aim of being integrated with CMOS and provide uniform SiNW with low line width roughness. SiNWs with widths down to 10 nm and low line width roughness of 1.5 nm has been achieved (see Fig. 5) using amorphous Si as the support material and standard CMOS process technology.

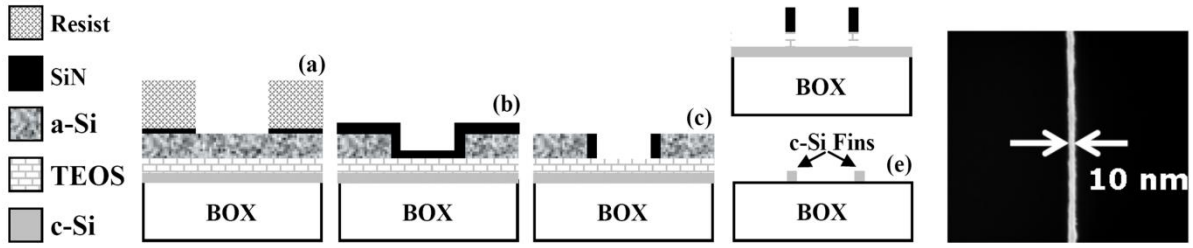

Fig. 5 Schematic of the STL process using an a-Si support layer to minimize the sidewall roughness. Top view SEM picture shows a 10 nm wide SINW by STL with LWR=1.5 nm (Nanofunction partner KTH).

Advanced nanopatterning, such as electron beam lithography and focused-ion beam lithography can write feature sizes below 10 nm; however, serial patterning is not practical for wafer-scale fabrication and equipment and operation is typically expensive. The essential advantage of this approach is the complete control over physical and electronic degrees of freedom. The geometry and alignment of the nanowire can be fully controlled by e-beam lithography and standard semiconductor processing techniques. Furthermore, physical gate electrodes next to the nanowire can be fabricated with complete control over their location and size [40]. These local gate electrodes enable controlled accumulation or depletion of surface charge carriers on the nanowire and provide the ability to tune the nanowire conductance necessary for the optimization of the detection sensitivity. At AMO and UCL top-down process platforms for fabrication of SiNW using high resolution e-beam lithography has been developed. At AMO NW FETs are fabricated in a top-down process using silicon-on-insulator (SOI) substrates. Single and multi-wire devices (see Fig. 6) with cross sectional dimensions down to 3 nm and gate lengths from 50 nm up to 100µm show an excellent switching behavior with a sub threshold swing down to S = 74mV/dec.

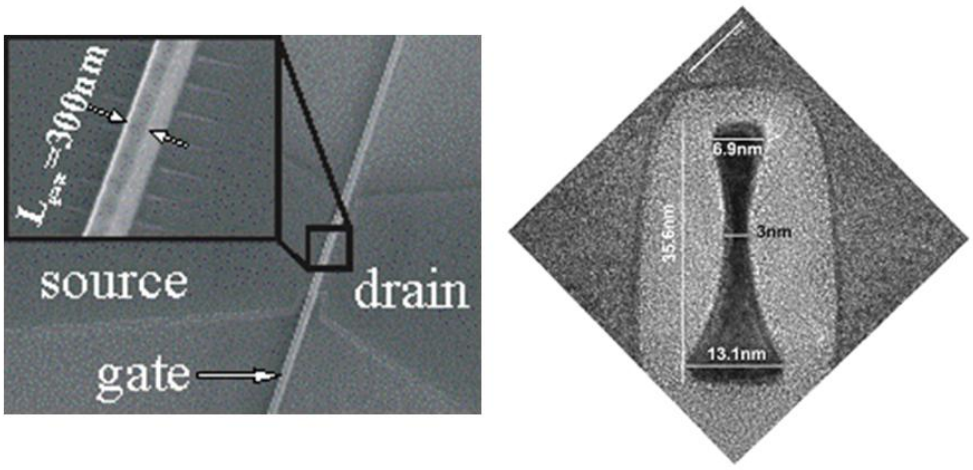

Fig. 6 SEM image of a SiNW FET (left) with 300 nm gate length and 12 parallell channels. At right a cross-sectional TEM image depicts a fabricated SiNW device (Nanofunction partner AMO).

N-type SiNW MOSFETs have been fabricated in a gate first process on SOI material (100) with silicon thicknesses of 20 nm and 10 nm and a boron doping level of 10^{15} cm^{-3}. The SiNWs have been patterned by electron beam lithography with an HSQ mask using a novel approach combining multi-pass grey scale electron beam lithography with proximity effect correction [59]. At UCL SiNW arrays (see Fig. 8) using e-beam lithography has been fabricated for gas detection (accepted for publication in IEEE Electron Device Letters).

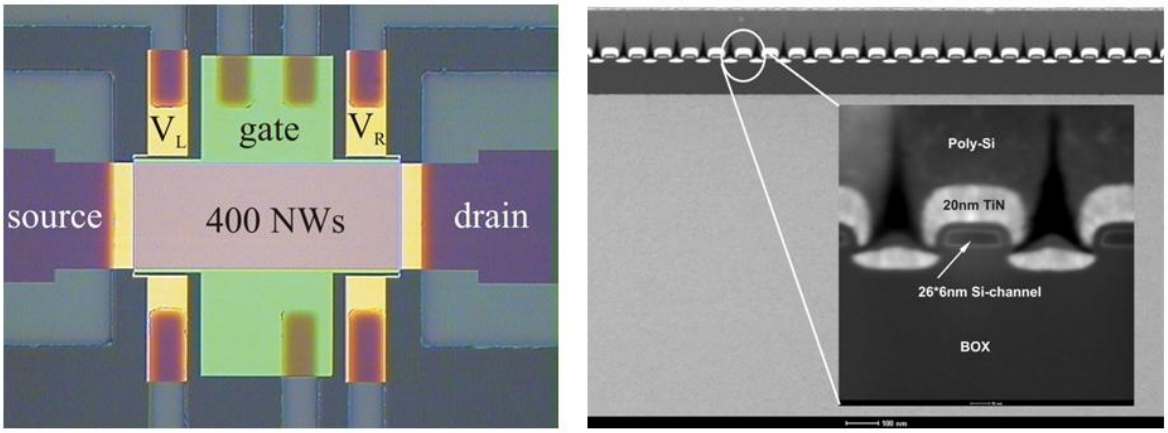

Fig. 7 Optical micrograph top view image (left) of a SOI SiNW nMOSFET with 400 SiNWs in parallel. To the right a TEM image shows cross section of the channel of a fully functional GdSiO/TiN nanowire n-MOSFET with sub-10 nm silicon channels (Nanofunction partner AMO).

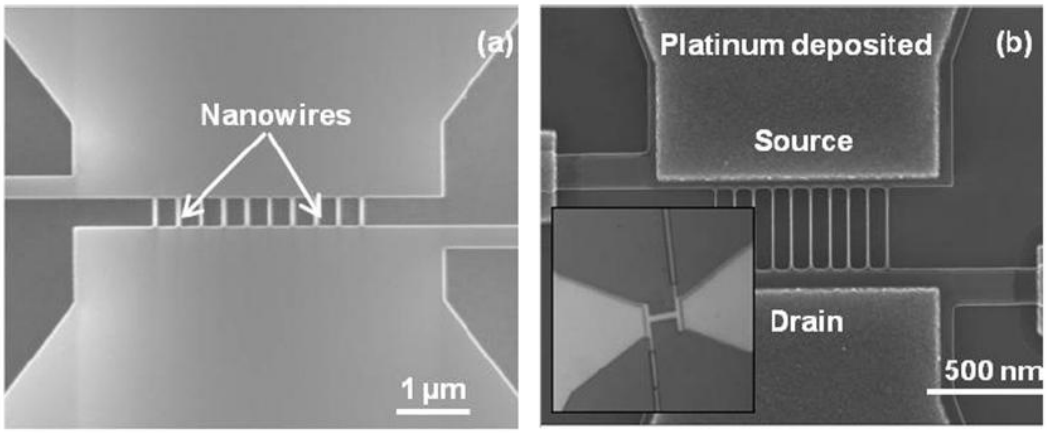

Fig. 8 Top-view SEM image of SiNW: (a) after resist development, (b) after lift-off of platinum on the source and drain pads (Nanofunction partner UCL).

3. Conclusions

Silicon nanowires can be fabricated with bottom-up and top-down approaches. The bottom-up approaches are often simple and can provide high density of NWs with high crystalline quality materials. We have shown that morphology and composition can be drastically improved using HCl in the Au catalyst growth of SiGe NWs. Although work has been progressing in recent years (e.g. FETs for sensors have been built) bottom-up approaches generally suffer from complex planar integration scheme for individual nanowires and it is difficult to predictably position many SiNW needed for a multifunctional sensor. Solutions involving large assembly of dispersed nanowires or direct integration of vertical NW arrays should therefore be preferred for low-cost sensors integration using bottom-up technologies. Top-down approaches have less severe integration issues with CMOS technology although electron beam lithography suffers from low throughput. In recent years advanced optical lithography and sidewall transfer lithography has improved and SiNW with dimensions in the 10-50 nm range can be fabricated with high throughput on wafer scale.

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