

Nano Packaging Technology for Interconnect and Heat Dissipation



May 2008

Newsletter #1

NANOPACK is a European FP7 large-scale integrating project aiming at the development of new technologies and materials for low thermal resistance interfaces and electrical interconnects, by exploring the capabilities offered by nanotechnologies and by using different enhancing contact formation mechanisms, compatible with high volume manufacturing technologies.

Thermal management of chip based electronic devices is becoming one of the largest bottlenecks to increased performance and integration density. Continued transistor downscaling is quickly reaching its limits forcing a new focus on heterogeneous integration and 3D packaging technologies to continue performance improvements by reducing interconnect length between memory and multi-core logic. Efforts must combine high density electrical interconnects with low resistance thermal interfaces to remove heat from the intricate layered assemblies. Power electronics applications in hybrid vehicles and power supplies are also being pushed to new integration densities that are largely limited by the ability to transfer heat across interfaces to liquid coolers and heat sinks. Improved thermal management and integration densities for these applications will also be important to improve energy efficiency and component reliability.

Focus

The most direct short-term technological result and economic benefit aimed by NANOPACK is a thermal interface system and process for power and microelectronics applications with revolutionary beneficial properties as urgently needed by industry.

NANOPACK has four major objectives:

- o Objective I: **Develop new interface technologies for low thermal and electrical resistance and discover new high-density integration technologies**
- o Objective II: **Develop new characterisation methods and tools for thin and highly conductive interface layers**
- o Objective III: **Use simulative and nano-analytical methods to understand heat transfer on a micro / nano scale**
- o Objective IV: **Build optimal demonstrators with respect to thermal, electrical and reliability-related properties to create impact in several industries**

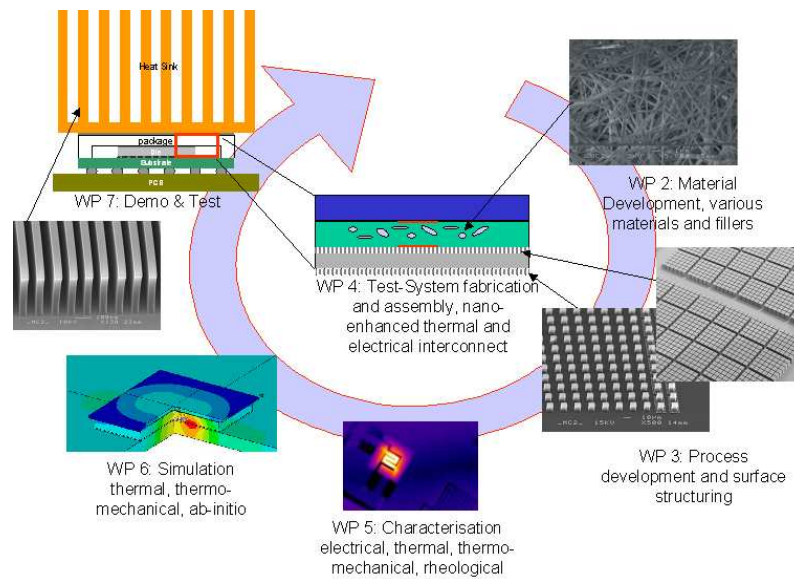
Presentation of the project activities

Material Development

Within the project, high performance nano-TIMs will be developed and manufactured. This can be accomplished by (i) finding out desirable nano-TIM compositions where nano-fillers and matrix may well be incorporated; (ii) by optimizing dispersing technologies to generate minimum thermal barriers between nano-fillers and matrix and to achieve a maximum thermal conductivity; (iii) by synthesizing nano-structured materials such as nanoparticles, nanotubes, nanofibrils packed nanoparticles and nanograss and (iv) by developing nano-porous resist templates for electroplated nano-structures. Thermal grease, thermal conductive adhesive, thermal conductive phase change materials and electrically conductive adhesive will be studied.

Process Development

These activities aim at establishing new manufacture and integration process which enables more efficient heat removal in modern integrated circuits and microsystems. Several parallel routes will be studied. A novel technique based on micromachined hierarchical nested channels (HNC) will be developed to modify the thermal interfaces, enabling the control of particle stacking during bondline assembly with highly particle-filled materials. High thermal conductive interconnects based on carbon nanotubes (CNT) and gold nano structures, which have much higher thermal conductivity than conventional materials, will be developed. These techniques also provide a possibility to build ultra fine pitch interconnection and thus allow very high integration density of microsystems.



Fabrication of Test Structures

The role of this work is to explore and manufacture test structures to facilitate the in-situ measurement of thin layers of very high thermal conductivity materials. Additional test structures will also be realised in order to investigate the electrical properties of microscale particle stacks for electrical interconnects in power electronics die attach. Both steady state and transient measurement methods will be used in the consortium.

Metrology and Characterization

This work is focused on the characterization of the interface materials along with their process dependence in thermal, electrical and thermo-mechanical properties. Test specimens will be measured in terms of thermal resistance, thermal conductivity/diffusivity, interface resistance and electrical conductivity, on a continuum or sub-micron scale, in static or transient modes, each of which has certain advantages with respect to sensitivity to a specific physical property, resolution or applicability. Failure and crack propagation will also be studied with advanced in-situ thermo-mechanical experiments.

Modelling and Simulations

State-of-the-art simulation techniques will be developed to better understand heat transfer at the nano and micro scales in thin films and dense particle systems. Both analytic techniques and IBM Blue Gene super-computer assisted molecular dynamics simulations will be used to explore phonon properties in nano scale systems. In addition to more scientific studies, traditional tools such as finite element analysis for mechanical structures will be incorporated for design of demonstrator devices and failure analysis.

Application demonstrators

With better cooling as developed in the NANOPACK project, electronic components can be packed more densely and be operated at higher power levels. This strongly increases the energy efficiency of the systems by reducing the need for chiller systems and limiting the waste of materials associated with lower density systems. The objective of this work is to exploit the newly enabled technologies by demonstrating several devices owning unprecedented thermal and electrical capabilities, in different fields of application.

Microprocessor



Automotive Electronics



Avionic Module



Off-shore cooling system



HP RF switch



System Specifications and State-of-the-Art

The WP1 “Systems and Applications Specifications” have successfully ended on-time at T₀+6 with the achievement of four deliverables¹ reviewing the material, environmental and functional specifications and requirements of the target applications (D1.1), defining evaluation vehicles (D1.2), establishing performance measurement methods (D1.3) and analysing the existing thermal and electrical interface technologies (D1.4). It has appeared for instance that a TIM verifying the following characteristics would satisfy most of the aimed applications: thermal conductivity between 10 and 20 W/mK and thermal resistance as low as 3 Kmm²/W for 30 µm of Bound Line Thickness.

Comparison and trade-off of existing TIM and interconnect alternatives

The deliverable D1.4 provides a comprehensive review of the recent progress of research work performed to develop new thermal interface materials. The review starts by classifying existing thermal interface materials and analyzing their advantages and disadvantages. Seven main classes of materials are examined, including thermal grease, thermal gel, phase change materials, phase change metallic alloys, thermally conductive adhesives, solders, thermal tapes and pads. The state-of-the-art research is then reviewed with an emphasis on those materials based on various carbon allotropes, such as graphite, carbon nanotubes and carbon fibres. The use of Carbon nanotubes as flip-chip interconnects is also assessed and the impact of microchannel surface modification is tackled.

Evaluation of commercial products

The deliverable D2.1 “Review and Evaluation Results of top TIMs used currently in Industry” provides a survey of the current literature, introduces the physics of thermal conductivity in particle filled materials, and summarizes the economic development of the field in the last decade. It then outlines the core features of the ASTM D5470 standard and the traditional test methods related to this standard in use at the different partners of the consortium. Next, a list of relevant materials is provided that summarizes the vendor provided thermal and electrical data along with the values that have been measured by the members of the Nanopack consortium. The state-of-the art exhibits thermal conductivity in the range of 3-5 W/mK and nominal thermal resistance of 15 Kmm²/W. Finally, the most relevant reference materials for our continued activities are discussed as well as the major shortfalls of the existing TIM materials. The data also show some shortfalls of current test equipment and justifies investments into improved metrology equipment in the different laboratories.

First nano-thermal grease

The milestone M2.1 of Work Package 2 “Development of Materials” of Nanopack has been achieved as planned in the project and has been presented in form of technical report at Nanopack meeting held on 28-29th of April 2008 in Gothenburg. “First Nano-Thermal Grease For Characterization And Modelling” as described in DoW has been prepared and is ready for further studies. In order to reach this milestone, a systematic experiments have been carried out to prepare carbon nanofiber/nanotube (CNF/CNT) based thermal greases including material selection and filler content determination, optimization of dispersion approaches and parameters, and measurement of thermal resistance. A number of carbon nanotube/fiber materials have been used to make thermal greases and their thermal performances have also been evaluated by measuring the thermal resistance. New CNF/CNT based thermal greases have been developed as the first milestone of this work package for characterization and modelling.

¹ Public deliverables can be requested by email to the project coordinator

NANOPACK at the THERMINIC Workshop!

NANOPACK will be first presented in detail to the thermal management community at the at the 14th International Workshop on Thermal Investigations of ICs and Systems, THERMINIC, that will be held in Rome Italy, 24-26 September 2008

<http://cmp.imag.fr/conferences/therminic2008/>



The workshop will feature a **special NANOPACK half day**. Within this half day 2 sessions are planned. The first one will give a short overview of the project itself to the international thermal management community. This session starts with a general presentation of the project, and will be continued by presenting the scientific results achieved so far within the project. The second session will include talks that are in close relation with the subject of the NANOPACK project, but not from NANOPACK authors. This session will give a very good opportunity to discuss and compare the different approaches, and will serve to gain new ideas to fine tune the ways to pursue in order to achieve the goals of the NANOPACK projects.

ESTC 2008

Chalmers University of Technology, member of the NANOPACK consortium, will attend the 2nd Electronics System integration Technology Conference, to be held in London, 1st-4th September 2008. Chalmers will present no less than five papers entitled:

- Overview of Carbon NanoTube for Electronic Interconnect
- Development of Heat Sink Performance of Microcooler Using Nanofluids Containing Carbon Nanotubes
- Electrical and thermal properties of electrically conductive adhesives using a heat-resistant epoxy binder
- Synthesis and Performance of Polymer-metal Nano-Composite as Thermal Interface Material for Thermal Management Applications
- Overview of Recent Progress of Thermal Interface Materials

The ESTC conference is dedicated to the fields of micro-electronics packaging and will tackle this year various topics such as Advanced Packaging Technologies, New Materials & Processes, Technology and Reliability for Nano and Micro Structures, Power Electronics, Manufacturing and Test Technologies, etc. Further information at <http://www.estc.biz/>

Remember to visit us at:

<http://www.nanopack.org/>



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Further Information at <http://www.nanopack.org/>