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Final proof-of-concept validation, results and analysis

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Abstract: This document describes the final integration and validation of the DUPLO proof-of-concept. DUPLO demonstrator combines different analog and digital self-interference cancellation techniques to enable full-duplex operation in compact commercially attractive radio communication devices. Two different DUPLO demonstrators targeting different compact form factors have been implemented. The first radio transceiver targets ultra small radio devices, such as smart phones. It integrates an electrical balance duplexer and a single-port planar inverted-F (PIFA) antenna. The second DUPLO radio node is compatible with integration in compact form factor devices such as small cell access points. This full-duplex transceiver includes a dual-polarized antenna and an active cancellation network at analog RF frequencies. Both DUPLO transceivers incorporate automatic tuning algorithms for the analog cancellation solutions which enable to dynamically adapt the analog cancellation blocks to the changes in the environment. Moreover, the DUPLO demonstrators also comprise a digital cancellation block which cancels the self-interference that remains after analog cancellation.

The DUPLO radio transceivers have been validated in a realistic dynamic indoor environment. The performance in terms of self-interference cancellation has been evaluated under different operating conditions. In addition, a full-duplex wireless point-to-point link has been demonstrated. Its performance in terms of error vector magnitude (EVM) and symbol error rate (SER) has been measured for different link distances, transmit powers and modulation schemes. All the obtained results have been included in this document, as well as the main finding gained from the validation and testing stage.

Executive Summary

This DUPLO deliverable D5.2 entitled "Final proof-of-concept validation, results and analysis" presents the final integration and validation of the DUPLO proof-of-concept. This document describes the final implementation of the key building blocks already reported in D5.1 [1], and their ultimate integration into the DUPLO radio node. Furthermore, the results obtained from the validation of DUPLO proof-of-concept are also included in this document.

DUPLO project investigates full-duplex technology for wireless communications transceivers as well as evaluates different radio resources management solutions for full-duplex wireless communications systems. By doing so, different full-duplex techniques have been investigated and evaluated across the DUPLO work packages, while, the DUPLO WP5 is in charge of integrating the different solutions into a common DUPLO demonstrator.

One of the key goals of the DUPLO project is to enable the application of full-duplex technology in 4G/WLAN and 5G systems. This entails the necessity of developing self-interference cancellation techniques which allow full-duplex operation in compact commercially attractive communication transceivers. However, these requirements are rather contradictory especially at analog level, since compact form-factor requirement reduces the physical space between transmitting and receiving antennas and circuits, which increase the self-interference. In fact, most of the state-of-the-art full-duplex radios rely on this physical spacing to achieve self-interference cancellation, as it was reported in deliverable D2.1 [2]. Nevertheless, DUPLO WP2 has developed two different analog self-interference cancellation techniques which can be implemented in compact radio devices. The first analog solution consists of an electrical balance duplexer, while the second analog SIC technique consists of a dual-polarized antenna and an active cancellation network.

As already reported in deliverable D5.1 [1], DUPLO WP5 has developed two different full-duplex demonstrators targeting two different compact form factors. Each full-duplex demonstrator integrates one of the analog techniques already mentioned, and also a digital cancellation block provided by DUPLO WP3. The first DUPLO demonstrator targets extremely compact form-factor devices such as smart phones or smart watches. It includes a single port compact antenna and the first prototype of the electrical balance duplexer (EBD) reported in deliverables D2.1 [2] and D5.1 [1], which provides a self-interference cancellation of 50 dB. The second DUPLO demonstrator is compatible with integration in compact form-factor radio transceivers such as small cell access points. This second demonstrator consists of a dual-polarized microstrip antenna in combination with an active cancellation network operating at RF frequencies. The total analog SIC provided by this combination is 60 dB. The second prototypes of the antenna and the active cancellation network reported in the deliverable D2.2 [3] have been used for integration in the final demonstrator. These second prototypes offer improved performance in terms of operational bandwidth and size with respect to the first prototyped solutions reported in deliverables D2.1 [2] and D5.1 [1].

Additionally, the two full-duplex radio nodes developed in DUPLO WP5 include automatic tuning algorithms for the analog solutions. These tuning algorithms allow to adapt the analog cancellation blocks to the changes in the environment close to the full-duplex transceiver, ensuring a good level of analog self-interference cancellation, i.e. more than 50 dB, over a wide range of scenarios. Moreover, both demonstrators also include digital cancellation algorithms provided by DUPLO WP3. This digital cancellation block utilizes a feed forward filter structure and has been implemented in MATLAB. It provides a digital self-interference cancellation of approximately 30 dB.

The hardware platform used for the integration of both demonstrators is the WARPv3 radio board. This radio board integrates a high performance FPGA, two flexible RF interfaces and multiple peripherals to facilitate rapid prototyping of custom wireless designs. The reference design used for both demonstrators is WARPLab v7.4 framework which enables PHY prototyping using WARP hardware for waveform transmission/reception and MATLAB for signal processing. By doing so, the arbitrary I/Q signals samples generated in MATLAB are sent to the WARP board via the Ethernet cable to their up-conversion and transmission. Likewise, the signals received by the WARP board are down-converted and transferred to MATLAB for post-processing.

The performance of both full-duplex radio transceivers has been experimentally validated by means of evaluating the self-interference cancellation performance over the complete system, and its adaptability to the dynamism of the wireless channel. Furthermore, an indoor full-duplex wireless link has been demonstrated for a variety of constellations up to 64QAM. The frequency channel used for the experiments has been 2.4GHz ISM band with a signal bandwidth of 20 MHz. The performance of the full-duplex wireless link in terms of EVM and symbol error rate has been measured, and the comparison with a half-duplex operation mode has been obtained and reported in this document.

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Acronyms and Abbreviations

ADC	analog to digital converter
ADSIC	analog and digital self-interference cancellation
AGC	automatic gain controller
ANT	antenna
ASIC	analog self-interference cancellation
BPSK	binary phase-shift keying
BW	bandwidth
C	capacitance
CDF	cumulative distribution function
CMOS	complementary metal oxide semiconductor
D	deliverable
DAC	digital to analog converter
dB	decibel
dBi	antenna gain in decibel referenced to isotropic antenna
dBm	power in decibels referenced to one milli-watt
DC	direct current
DUPLO	full-duplex radios for local access project
EBD	electrical balance duplexer
EVM	error vector magnitude
FD	full duplex
FDAC	full duplex analog cancellation
FDADC	full duplex analog and digital cancellation
FDD	frequency division duplex
FFT	fast Fourier transform
FPGA	field-programmable gate array
GHz	giga (10^9) Hertz
HD	half duplex
I/O	input/output
IC	integrated circuit
IEEE	institute of Electrical and Electronics Engineers
IP	Internet Protocol
JSAC	Journal on selected areas in communications
LNA	low noise amplifier
LO	local oscillator
LTS	long training sequence
MAC	medium access control
Mbits/s, Mbps	mega bits per second
MHz	mega (10^6) Hertz
MOD	modulator

NoC	network on chip
OFDM	orthogonal frequency-division multiplexing
PA	power amplifier
PC	personal computer
PCB	printed circuit board
PIFA	planar Inverted-F Antenna
PTX	transmit power
QAM	quadrature amplitude modulation
QPSK	quadrature phase-shift keying
R	resistor
RF	radio frequency
RFIC	radio frequency integrated circuit
RSSI	received signal strength indicator
RX	receiver
SAW	surface acoustic wave
SER	symbol error rate
SI	self-interference
SIC	self-interference cancellation
SIR	signal to interference ratio
SMA	sub-miniature version A
SNR	signal to noise ratio
SoC	system on chip
SOTA	state of the art
STS	short training sequence
TDD	time division duplex
TRX	transceiver
TX	transmitter
UDP	user datagram protocol
USB	universal serial bus
VM	vector modulator
VSWR	voltage standing wave ratio
WARP	wireless open-access research
WLAN	wireless local area network
WP	work package
XPD	cross polar discrimination
Zant	antenna impedance
Zbal	balance network impedance

1. INTRODUCTION

The rapid growth of mobile communications as well as the demand from subscribers for better mobile broadband experiences is encouraging the industry to look ahead at how networks can be developed to meet future extreme capacity and performance demands. The 3G and 4G mobile broadband technologies have mainly focused on providing mobile video, web/data, music and file sharing. However, this will continue through the future 5G systems which will offer enhances capacity, higher data rates and wireless access to all, driven by highly advances applications and services. Taking into account these demanding requirements, full-duplex (FD) communication is considered a way to potentially double the speed of wireless communications and can be considered a key technique for future 5G systems.

Full-duplex transmission is a potential air interface technique which can theoretically double the spectral efficiency in terms of transmitted bits per second per Hz. Moreover, full-duplex technology offers also improvements at higher layers such as the elimination of hidden terminals. However, achieving full-duplex communication involves solving many technical challenges related with the radio transceiver implementation. The primary challenge is the strong self-interference (SI) that leaks into de receiver from its own transmitter. The self-interference cancellation requirement for a full-duplex radio transceiver can be more than 100 dB [2], however, considering small area scenarios, full-duplex transmission can improve the system capacity over half-duplex transmission even for 70-90 dB of SIC as deliverable D4.1 [4] reports.

In order to achieve such self-interference cancellation requirement, different cancellation techniques should be implemented at different stages of the full-duplex transceiver, combining different antenna isolation, analog and digital cancellation techniques. DUPLO project investigates full-duplex technology for wireless communications transceivers as well as evaluates different radio resources management solutions for full-duplex systems. With this regard, different self-interference cancellation techniques have been evaluated across the DUPLO work packages and a final DUPLO demonstrator has been implemented and validated in DUPLO WP5.

The DUPLO project identified and quantified the main design requirements over the targeted network types and scenarios within the framework of DUPLO WP1 [5], therefore these requirements were considered for the design of the different key building blocks. One of the requirements identified consists of the necessity of developing self-interference cancellation solutions compatible with its integration in compact transceivers. However, compact form-factor requirement reduces the physical space between transmitter and receiver which can increase the self-interference. In fact, most of the state-of-the-art full-duplex works rely on the physical spacing between transmitter and receiver or on the use of multiple antennas to achieve self-interference cancellation, which hamper dense and cost-efficient integration [2]. Nevertheless, the SIC solutions developed by DUPLO WP2 provide good level of self-interference at analog RF level and compact form-factor simultaneously. These analog solutions have been already described in deliverables D2.1 [2] and D2.2 [3] and in JSAC paper publication [6]. These analog blocks have been integrated in the DUPLO demonstrator together with digital cancellation algorithms provided by DUPLO WP3, in order to achieve the SIC required for small cell scenarios.

DUPLO WP5 has integrated two different full-duplex demonstrators which target different compact form factors. Each demonstrator integrates one of the SIC solutions developed in the framework of DUPLO WP2. The first full-duplex demonstrator targets ultra small radio devices such as smart phones or smart watches. It integrates an RF circuit transceiver which acts as a duplexer interconnecting the RF transmitter and receiver ports with a single port antenna. This duplexer is implemented as an electrical balance circuit processed in plain CMOS technology. The duplexer consists of an on-chip transformer and a tunable balance network. The balance network matches dynamically the antenna impedance over different environmental conditions providing 50 dB of self-interference suppression before the LNA. Furthermore an automatic tuning algorithm has also been developed in MATLAB to automatically adapt the balance network to the antenna impedance.

The second implemented DUPLO demonstrator is compatible with compact radio devices such as small cell access points. This full-duplex radio transceiver consists of a dual-polarized microstrip antenna which provides more than 50 dB of self-interference isolation by means of using orthogonal polarizations for transmission and reception. However, nearby objects close to the dual-polarized antenna can degrade the antenna isolation causing the saturation of the receiver. Therefore, the dual-polarized antenna is combined with an active cancellation network which operates at analog RF frequencies. This active cancellation enables to combine an attenuated and phase shifted copy of the transmitted signal to the self-interference that leaks from the antenna. By doing so, the active cancellation dynamically adapts to the environmental conditions close to the antenna maintaining the analog self-interference cancellation above 50 dB. Moreover, an automatic tuning algorithm has been implemented in a microcontroller to dynamically adapt the attenuation and phase shift coefficients of the active cancellation network.

The analog SIC solutions abovementioned have been combined with a digital cancellation block to achieve the required 70-90 dB of total SIC. The digital cancellation algorithms have been implemented in MATLAB as a feed forward filter. Two different digital baseband SIC methods are used depending on the time synchronization of the received and self-interference signals. If SI and received signal are time synchronized then frequency domain cancellation gives the best performance while time domain cancellation provides better results when signals are not time aligned.

Both developed demonstrators have been integrated using WARPv3 radio board and WARPLab v7.4 framework. This WARPLab framework has replaced the OFDM reference design originally planned for the integration, due to the critical changes required by the OFDM reference design to enable full-duplex transmission. Moreover, OFDM reference design does not allow to capture I/Q signals samples while WARPLab framework enables PHY prototyping using WARP hardware for waveform transmission/reception and MATLAB for signal processing. This way, this new framework provides an efficient way to implement and validate the full-duplex proof-of-concept, as well as to quantify the self-interference cancellation performance over real environments.

This document reports the final integration and validation of the different key building blocks already introduced in DUPLO deliverable D5.1 [1]. Section 2 gives an overview of the final architecture implemented in both DUPLO demonstrators. The final prototypes implementation and their stand-alone validation are included in section 3. DUPLO demonstrator has been experimentally validated in an indoor environment. With this regard, the self-interference cancellation performance over the complete system has been evaluated. Moreover, DUPLO WP5 has demonstrated an indoor full-duplex wireless communication link for a variety of constellations up to 64 QAM. The frequency channel selected for the experiments has been 2.4GHz ISM band with a signal bandwidth of 20 MHz. The performance of the full-duplex link over different conditions and scenarios and the obtained results are included in the section 4. Section 5 gives an analysis of the results obtained from the DUPLO proof-of-concept, while main conclusions are reported in section 6.

2. FULL-DUPLEX DEMONSTRATOR FINAL ARCHITECTURE

The DUPLO project has identified and quantified the main design requirements over the targeted networks types and scenarios [4], [5], [7]. Based on this analysis, DUPLO project has identified small cells as one of the main areas of interest for the project, due to their relevance for future 5G networks, as well as because small areas with short link distances and low transmission powers forms feasible deployment scenario for full-duplex technology. Due to these reasons, a small cell indoor scenario has been selected for the DUPLO proof-of-concept.

The analysis developed in the framework of DUPLO WP1 and WP4 concluded that in small area systems full-duplex transmission can provide system level performance gains over half-duplex with a self-interference cancellation level of 70-90 dB, although better self-interference cancellation capability in the full-duplex transceiver would be beneficial in expanding the competitive operation range of full-duplex transmission. To satisfy this requirement in terms of self-interference mitigation, DUPLO demonstrator implements different analog and digital self-interference cancellation techniques at different stages of the full-duplex transceiver.

DUPLO WP2 has been focused on the investigation of novel self-interference cancellation techniques which are commercially attractive in terms of form-factor, system integration and operation flexibility. The analog self-interference cancellation solutions investigated in this DUPLO WP2 have been integrated together with digital cancellation block provided by DUPLO WP3 into two different compact form-factor demonstrators:

- Single-port antenna demonstrator: This radio node targets extremely compact form-factor radio devices such as smart phones or wearable technology. The radio transceiver consists of an electrical balance duplexer processed in plain CMOS technology and a single-port PIFA antenna. The balance network adapts to the antenna impedance over different operational scenarios to achieve self-interference suppression from the transmitter to the receiver. This analog cancellation block is combined with digital cancellation algorithms to satisfy the required level of SIC.
- Dual-port antenna demonstrator: This radio transceiver is integrated by a dual-polarized antenna which operates with orthogonal polarizations in transmission and reception to achieve self-interference isolation at antenna level. Additionally, the dual-polarized antenna is combined with an active cancellation network to compensate the effects of objects close to the antenna, which can degrade the antenna isolation. As in the case of the single-port antenna radio node, the dual-polarized antenna and the active cancellation network are combined with digital cancellation algorithms.

Both demonstrators are able of adapting to the environmental changes close to the antenna by means of implementing automatic tuning algorithms over the analog circuitries. Moreover, the demonstrators are integrated in WARPv3 radio board using WARPLab framework.

This section describes the final architecture of both demonstrators (which has suffered some modifications with respect to the architectures reported in deliverable D5.1 [1]). The main building blocks of DUPLO demonstrators are described in this section as well as the main interfaces between these key building blocks.

2.1. SINGLE-PORT ANTENNA RADIO NODE

In the DUPLO project, a solution has been developed which enables the usage of a single-port antenna in a full-duplex radio node. This approach is very attractive from a commercial point of view, as this allows to use commercial off-the-shelf antennas which are developed for legacy communications such as half-duplex (HD) and frequency-division duplexing (FDD). Such antennas are typically optimized in cost and size, and they are already available in existing radio devices. Adding the full-duplex functionality to existing radio devices could allow to share the antenna between the different transmission schemes, enabling compact integration.

The RF circuit enabling the usage of a single-port antenna for full-duplex operation proposed in WP2 of the DUPLO project is the electrical balance duplexer (EBD). The term ‘duplexer’ is generally known from FDD, where the duplexer enables to use a single-port antenna for simultaneous transmission and reception. Such

duplexers are generally surface-acoustic wave (SAW)-based components to prevent the transmitted signal and TX-generated noise at the RX frequency from leaking into the RX. SAW-duplexers can exploit the frequency difference between the two FDD-signals and use filtering to prevent leakage. In FD, this operation principle cannot be applied as there is no frequency separation.

The EBD established a self-interference cancellation even when there is no frequency separation between the TX and RX. The electrical-balance duplexer operation principle is illustrated in FIGURE 1; the RF circuit comprises a hybrid transformer and a balance network which is essentially a tunable dummy load impedance. By tuning the balance network impedance, the magnitude and phase of two TX-RX transfer paths are made equal, such that they destructively interfere at the RX port. This hybrid junction circuit provides an attractive duplexing performance for FD, and can be densely implemented in CMOS technology and can be co-integrated with the transceiver circuitry [2]-[3].

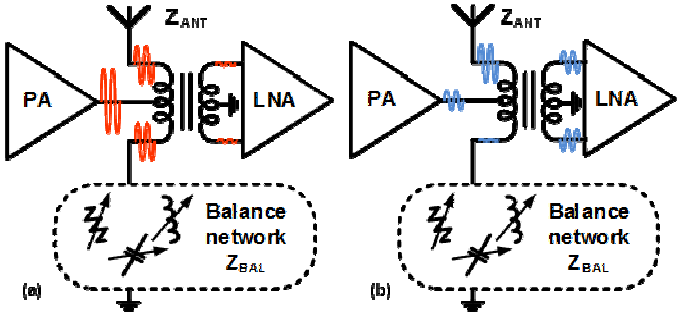


FIGURE 1. Electrical balance operating principle for (a) TX operation and (b) RX operation: in FD, (a) and (b) occur *at the same time and frequency*.

In D2.1 and D2.2, two EBD designs have been presented. In order to maintain the project timeline, the first design has been considered for the proof-of-concept integrated demonstrator. The main characteristics of this design related to this document are:

- Balance network consisting of an R/C network, offering independent tuning of R and C.
- Moderate impedance coverage offered by the balance network.
- Extremely high narrow-bandwidth SIC performance, but decreasing average SIC performance for increasing bandwidth.
- Differential RX output offering differential SIC, but may cause a common-mode SI and prevents a high-power operation.
- SI-induced distortion in the balance network leaking to the RX with high-power operation.

These characteristics and the corresponding values are reported in [2] and [3].The main shortcoming have been addressed in the second design [3], but are out of scope of DUPLO WP5.

FIGURE 2 shows the radio node architecture, where the single port antenna is directly connected to the tunable RF circuit. This single antenna is used both for transmission and reception. The electrical balance circuit interfaces between the single port antenna and the RF ports of WARP, and isolates the received signals from the transmitted signals. On WARP, one RF interface is configured as transmitter and another is configured as receiver. The digital signal processing, MAC processing and digital cancellation algorithms could be implemented in the Virtex-6 FPGA of the WARP platform, but this has not been done in the frame of this project. All digital processing has been performed in MATLAB; the WARPLab v7.4 framework was used to perform data acquisition by means of WARPv3, while the main signal processing such as the tuning algorithm, the digital cancellation, and the processing of the signal frames are done on the PC. A modified version (as explained in section 3.3) of IEEE802.11 standard are used with channels of 20MHz bandwidth (or less when indicated) in the 2.4GHz ISM band.

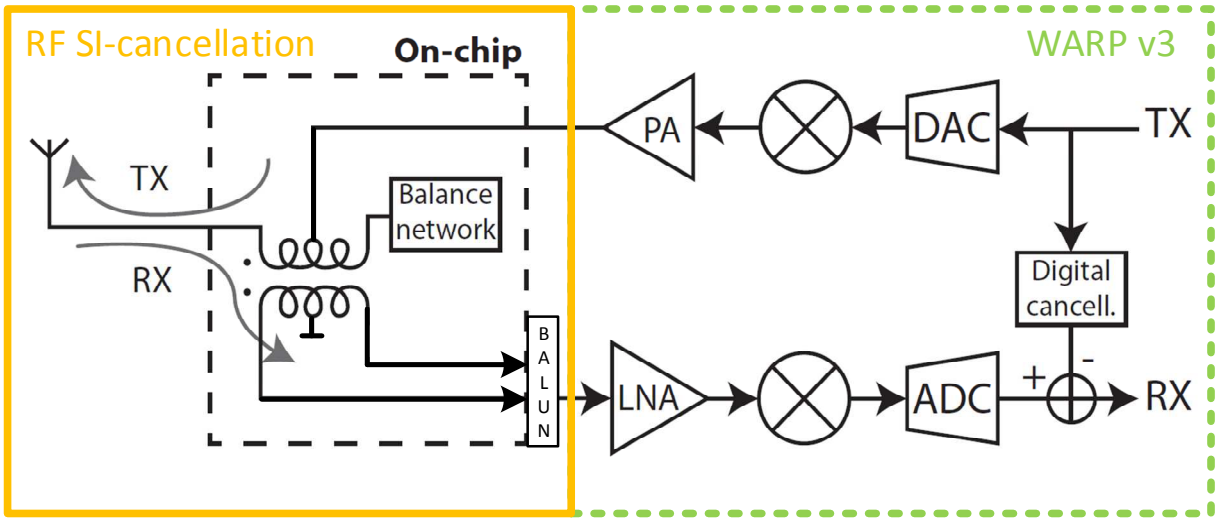


FIGURE 2. Single port antenna radio node architecture.

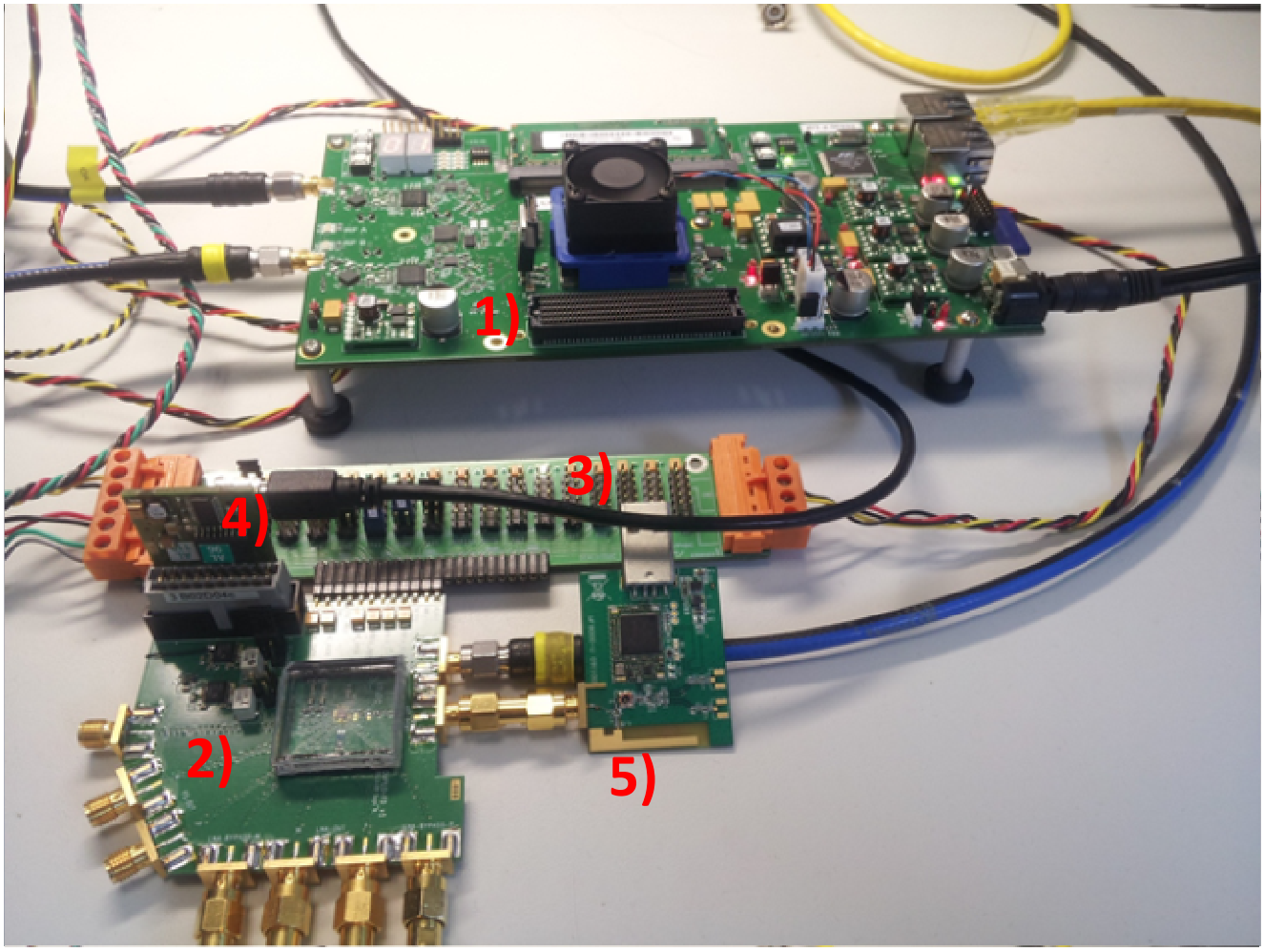


FIGURE 3. Picture of the full-duplex single-port antenna experimentation setup including WARPv3 and tunable duplexer.

FIGURE 3 shows the experimentation setup of the single port antenna radio node.

1) WARPv3

WARPv3 is controlled by MATLAB via the Ethernet connection, and the FPGA embeds WARPLab 7.4. This enables a seamless connection between MATLAB and WARP for control and IQ data exchange. In this setup the two RF interfaces on the WARPv3 main PCB are used. One of these interfaces is configured as transmitter and the other as receiver. WARP is using channels in the 2.4GHz ISM band. Note that the TX and RX path of a single WARP platform operates on a different local oscillator. Therefore, the phase noise of the TX and RX will be uncorrelated. This will limit the maximal achievable full duplex SI-cancelling performance [8].

2) Tunable EBD module

The EBD RFIC is mounted on this module via direct chip bonding. The module has a diversity of connectors:

- RF interface via SMA connectors: apart from the antenna and transmitter connection, the receiver can be connected differentially with or without inclusion of the on-chip LNA. This LNA improves the receiver noise figure, and the bypass option enables to characterize the electrical balance without this amplification stage.
- Power supply connections: the RFIC building blocks are supplied with dedicated supply connections. This results in a bus of supply lines. The power supply board supplies the supply lines efficiently. There are two main supply voltages: 3.3V for the digital I/O ring and 1.8V for both the digital and analog circuits.
- R tuning: unlike the C-tuning, the on-chip resistor of the balance network is directly tuned by means of an analog voltage. To enable digital control via the serial control interface, a DAC has been implemented on the EBD module which translates the digital code provided by the serial control interface to an analog tuning voltage.
- Serial control interface: the tunable balance duplexer module is controlled by means of a serial shift register. This shift register controls the components on the PCB (e.g. discrete DAC), the on-chip capacitor setting and the chip configuration.

3) Power supply board

This power supply board has de ability to route and distribute different supply voltages by manual setting of the jumpers. Redistribution of the supply voltages is not needed. External power supply sources are connected to the power supply board.

4) Serial control module

The serial control module is a custom-designed PCB which enables communication from MATLAB to the shift register via USB. The serial control module performs the necessary data translation and takes care of the USB protocol.

5) Antenna

An antenna from a commercial USB WiFi module has been used. This WiFi module has been hacked to connect directly to the antenna itself, bypassing all the hardware on this WiFi module. The antenna has a planar inverted-F patch (PIFA) structure, and has only one connector port.

As the solution discussed in this section targets integration in extremely compact radio devices, one should avoid additional hardware or circuitry to perform secondary tasks. It could be, for example, convenient to implement a power detector at the receiver input to monitor the self-interference isolation of the tunable duplexer. Given the high integration target, all monitoring and tuning activities will be performed at baseband without additional RF circuits. This implies however that no specific measures of the tunable duplexer are

available during operation; the measures will cover a combination of baseband and RF behaviour. The tuning algorithms are discussed in section 3.1.

The single-port antenna radio node has been used in two validation setups which will be described in sections 2.3 and 4:

- The first test setup implements a single radio node. This setup enables to validate the EBD performance in conjunction with WARP and to implement and test e.g. tuning algorithms based on different environmental conditions. The stand-alone EBD performance measured with WARP and/or with test and measurement equipment has been reported partially in deliverables D2.1 [2], D2.2 [3] and D5.1 [1]. Additional results are described in section 3.1.
- The second test setup implements two FD radio nodes which communicate via a full-duplex wireless point-to-point link.

2.2. DUAL-PORT ANTENNA RADIO NODE

The architecture of the dual-port antenna radio node was already introduced in the deliverable D5.1 [1]. However, some modifications have been included in the final architecture of the demonstrator, which are reported in this deliverable D5.2. FIGURE 4 illustrates the different key building blocks which integrate the dual-port antenna radio transceiver. As can be seen from this figure, the radio node consists of:

- Dual-polarized antenna: This is a dual-port planar microstrip antenna which operates with orthogonal polarizations for transmission and reception. The use of this orthogonal polarizations provides a self-interference suppression at antenna level of more than 50 dB as will be shown later in this document. The antenna has two ports which are respectively connected to the transmission and reception paths by means of using SMA connectors.
- Active Cancellation Network: This active cancellation network provides self-interference cancellation at analog RF frequencies. The cancellation network takes a copy of the TX signal to apply a variable attenuation and a variable phase rotation. Then, the cancellation network combines this attenuated and phase-shifted copy of the TX signal with the self-interference that leaks from the dual-polarized antenna. The objective of the cancellation network is to compensate the environmental effects that can degrade the antenna self-interference suppression, and maintain the self-interference cancellation before the receiver LNA better than 50 dB. Furthermore, the active cancellation network includes a self-interference power detector. This power detector monitors the power of the self-interference signal after the active cancellation network and uses this power as the input for a gradient descent algorithm. This algorithm finds the settings of the attenuation and phase shift which minimize the residual self-interference signal after the active cancellation. The algorithm can dynamically adapt the attenuation/phase coefficients to the changes in the environment, maintaining the analog SIC above a predefined threshold for a wide range of operational conditions. The active cancellation board is controlled from an external control unit (STM32F4 microcontroller) which also implements the gradient descent algorithm, as will be shown in section 3.2.2.
- WARPv3 radio board: The WARPv3 radio board has been also used for the integration of the dual-port antenna transceiver . The settings of the WARP transmitter and receptor, i.e. frequency channel, gain of the amplifiers, type of constellation, etc., are defined from a control PC which is connected to the WARP board via the Ethernet line. The channel used for this DUPLO demonstrator is 2.45 GHz band, i.e. channel 10 of WARPv3, while the signal bandwidth is 20 MHz. With regard for the reference design, WARPLab v7.4 framework has been also used for the integration, as section 2.3 describes.
- Digital Cancellation block: The digital cancellation block cancels the remaining self-interference up to the receiver noise floor by means of applying cancellation algorithms in the baseband domain. It takes the I/Q signals samples that are transmitted/sent to/from the WARP and applies a feed forward filter in order to cancel the self-interference signal.

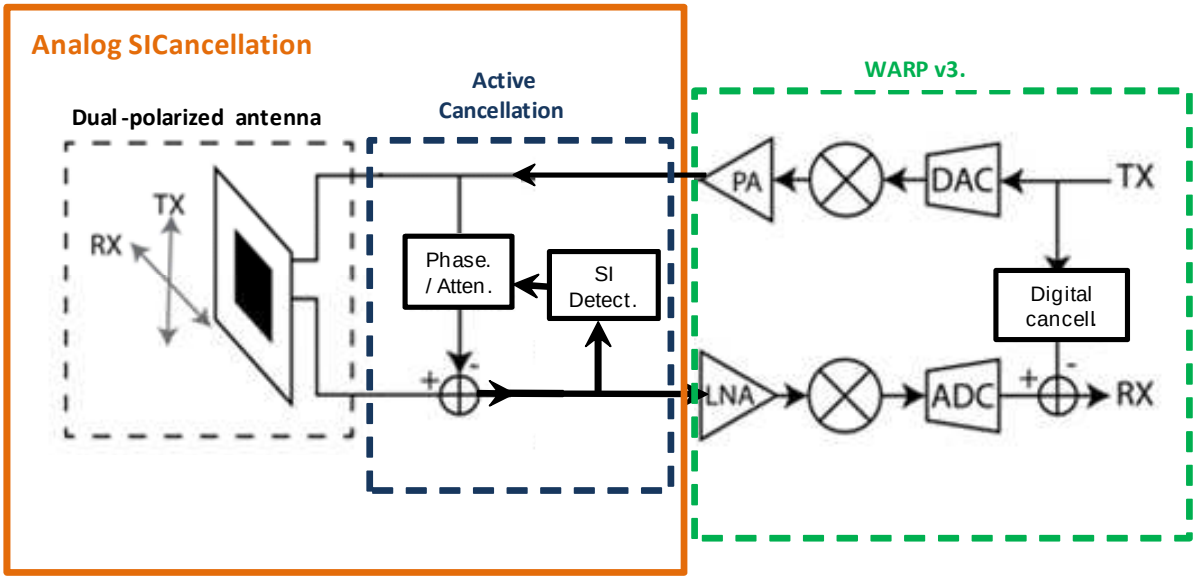


FIGURE 4. Dual-port antenna radio node architecture.

FIGURE 5 shows a picture of the dual-polarized antenna radio node. The abovementioned key building blocks can be shown is this figure as well as the external control unit used to control the settings of the active cancellation network. The transmission and reception RF paths are connected via SMA connectors and RF cables, and external power supply is used to power the active cancellation network. The interfaces defined among the key blocks will be more detailed described in section 3.2.3.

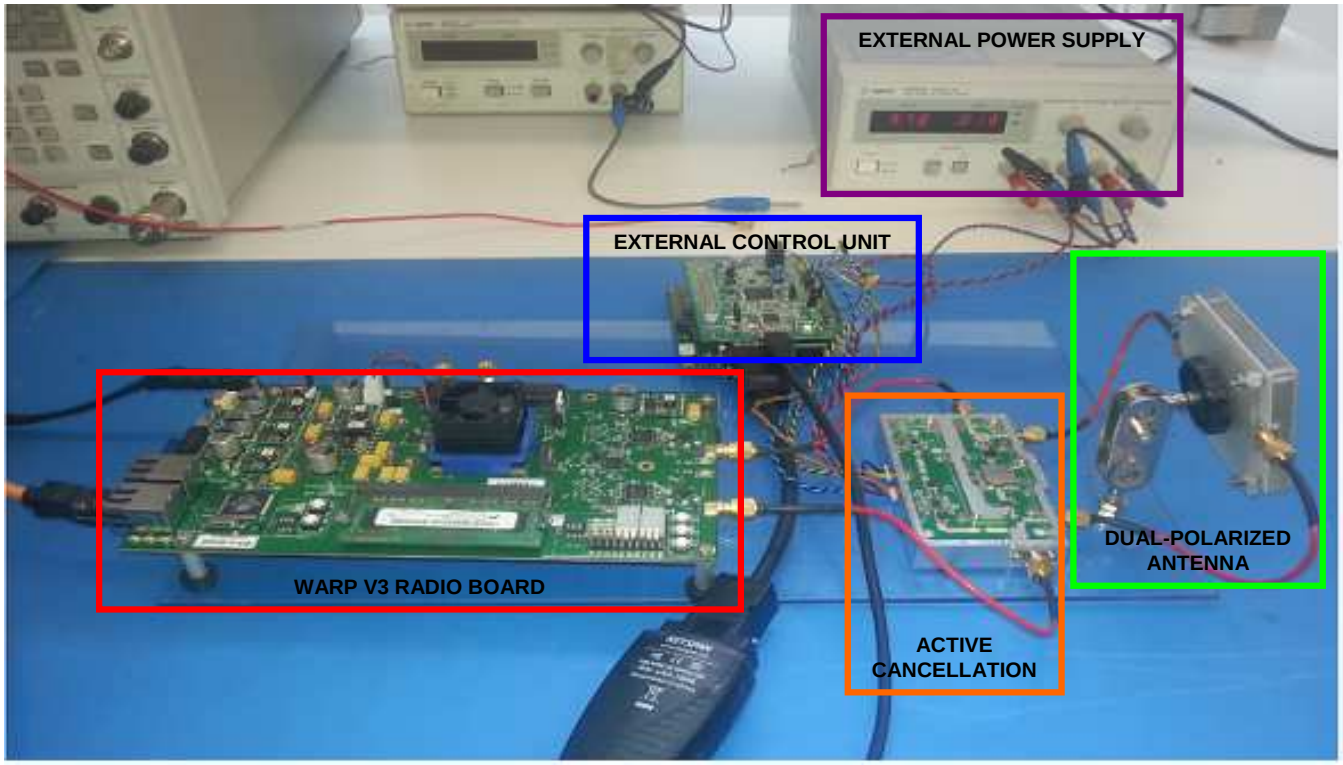


FIGURE 5. Picture of the dual-port antenna radio node.

FIGURE 6 illustrates the graphical user interface (GUI) developed to control the settings of the dual-port antenna demonstrator (both radio transceiver nodes). This GUI has been developed in MATLAB and allows to set some parameters of the WARP radio board such as the channel, transmit power or modulation scheme.

Moreover, the user interface permits to obtain information of the active cancellation network. In particular, the values of the attenuation and phase shift that minimize the self-interference signal. Additionally, the MATLAB GUI is also used for results visualization and data analysis as will be shown in section 4.

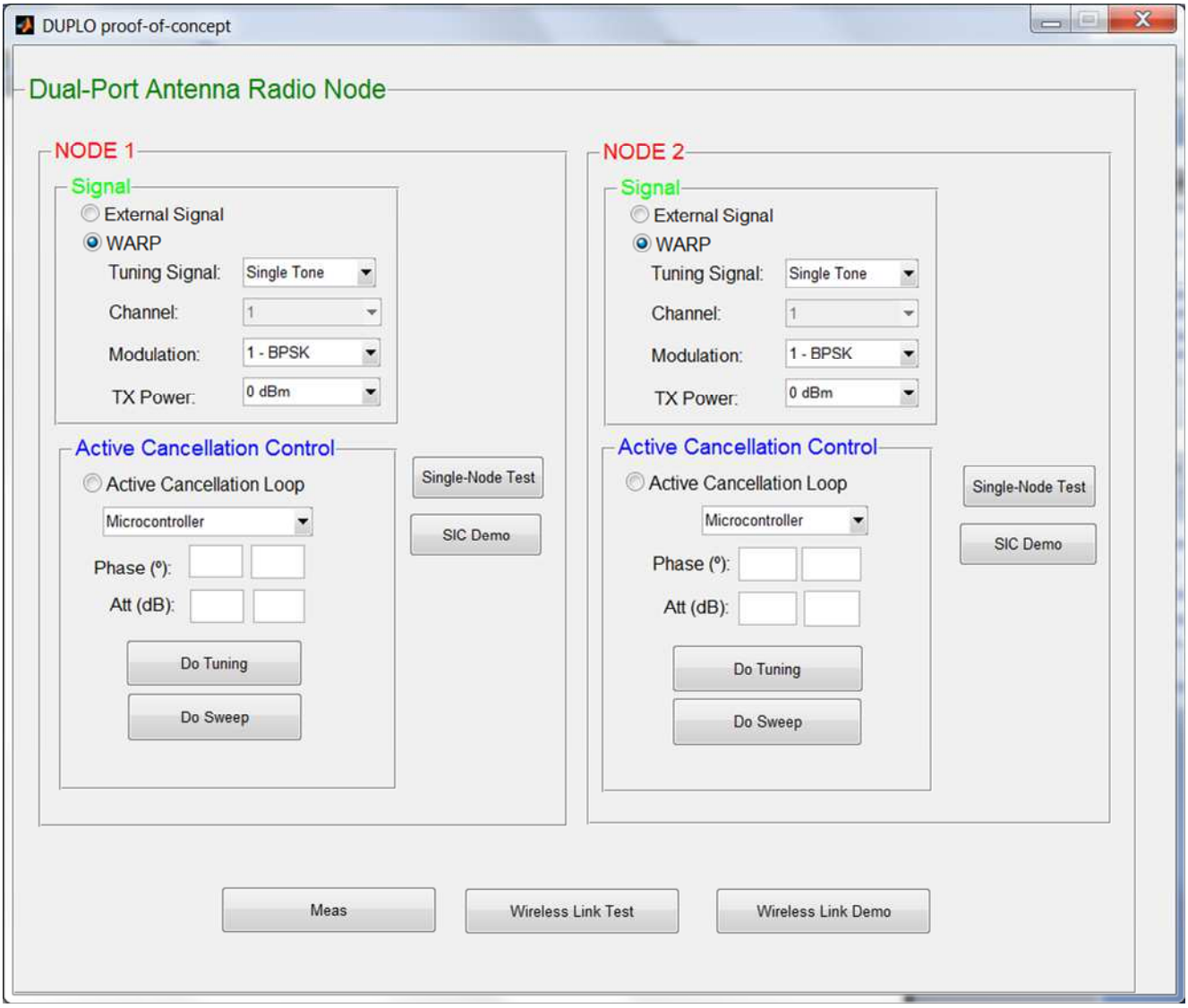


FIGURE 6. Graphical User Interface for dual-port antenna demonstrator control and validation.

2.3. INTEGRATION PLATFORM

As already mentioned, WARP version three hardware platform [9] is being used for both DUPLO demonstrators. The technical specifications of this WARP radio board and its main features were reported in deliverable D5.1 [1]. Additionally, the reference design being used for the demonstrator is called WARPLab [10], [11]. This framework allows to control various hardware blocks of the WARP radio board like transmit and receive amplifiers, AGC, etc. by using MATLAB. Furthermore, it allows generating arbitrary I/Q samples in MATLAB which can be up-converted to the desired frequency and transmitted through WARP TX port. Similar processing can be done at the receiver side, where received RF signal is down-converted and the I/Q samples are transferred to MATLAB via the Ethernet line for further processing. As the signal processing can be done at MATLAB, this framework allows to develop baseband algorithm in a relative easy way.

Another framework which can be used with WARP hardware is known as OFDM reference design [12]. This framework implements the digital modem and baseband along with other needed controllers in the Xilinx Virtex-6 LX240T FPGA integrated in the WARPv3. However, this is inherently a half-duplex design, meaning it

deliberately turns off all the receiver state machines in case transmission is happening and vice-versa. This framework was initially planned to be used for the DUPLO demonstrator. Therefore, to use this design for DUPLO proof-of-concept meant not only to break those dependencies but to also incorporate multitude of system changes like modified frame structure, while making sure that the necessary blocks like channel estimation and equalization work with those changes. Furthermore, as the original design runs in a pipelined manner, it had to be made sure that full-duplex demonstrator related modifications did not break the tightly coupled pipeline. Additionally, the framework did not allow to capture I/Q samples from the hardware and process them offline in MATLAB. Due to these challenges, it was decided to replace this OFDM reference design by the WARPLab 7.4 framework, which is currently used in the final DUPLO proof-of-concept.

The decision to use WARPLab instead of the OFDM reference design introduces latency problems. The round trip time between two computers connected to two separate WARP nodes which are running OFDM reference design is of the order of few milliseconds. However, the same latency when measured using WARPLab design is about two order higher. This delay is caused by the involvement of the MATLAB at both sides and it will vary highly depending upon the processing power available. This uncertainty and delay makes the throughput metric highly unreliable, and this is the reason why this metric has not been evaluated with the demonstrator. Contrarily, this limitation does not have any impact on demonstrating the adaptation capabilities of the analog and digital cancellation blocks whit time varying wireless channel, as well as it allows also to evaluate the full-duplex link performance.

Two different types of demonstration setups have been developed for the DUPLO proof-of-concept as will be shown later in section 4. On one hand, a single full-duplex radio node is used to evaluate the cancellation capabilities over the different analog and digital stages. In this setup, the received signal at digital baseband consists of self-interference and noise. The analog cancellation stages are tuned separately. Before any signal is received, the receiver gains are fixed according to the transmitted power. The metric provided by this setup is the self-interference cancellation capability in decibels achieved at analog and digital levels. At analog domain the self-interference is calculated by measuring the RSSI of the received signal frame. WARPv3 uses a 10-bit ADC for RSSI measurement in WARP transceiver (Maxim MAX2829 [13]). This value is measured from WARPLab and converted to dBm taking into account the gain settings of the receiver amplifier. Finally, the analog self-interference cancellation is calculated with the power of the transmitted signal and the measured level of RSSI .With regard to the digital domain, the self-interference cancellation is calculated as

$$SIC_D = 10\log_{10}\left(\frac{P_{SI}}{P_N}\right) \tag{1}$$

where SIC_D represents the digital self-interference cancellation, P_{SI} is the SI power after digital cancellation and P_N is the noise power. The position of noise samples and self-interference samples is shown in the FIGURE 7.

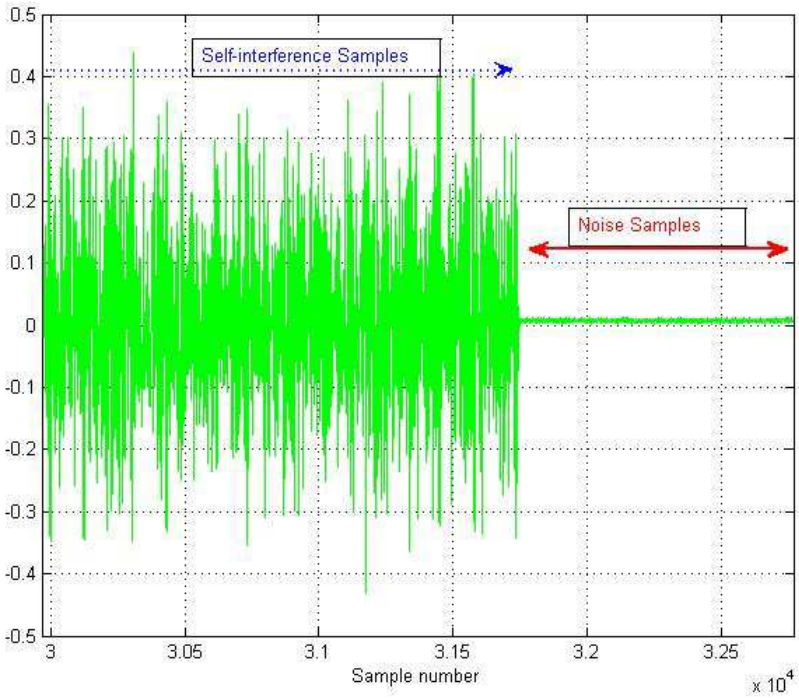


FIGURE 7. Self-Interference and noise samples.

On the second hand, a dual node setup is employed to evaluate the performance of the full-duplex wireless link, as well as it capabilities. This setup consists of two full-duplex radio nodes separated a certain distance and operating both nodes in full-duplex mode. It provides quantifiable metrics to evaluate the full-duplex link performance and comparing it with a half-duplex link. Moreover, it also demonstrates the adaptive nature of the analog cancellation stages. FIGURE 8 shows the flow diagram for the dual node setup. The first step is initializing the WARP hardware. It includes setting gains of transmit amplifiers, setting appropriate channel and initializing few MATLAB structure. The link is operated for a predefined number of frame transmission counts. There is no limitation on the number of frames; however there is a limitation on the maximum size of one frame. Currently this is about 819us.

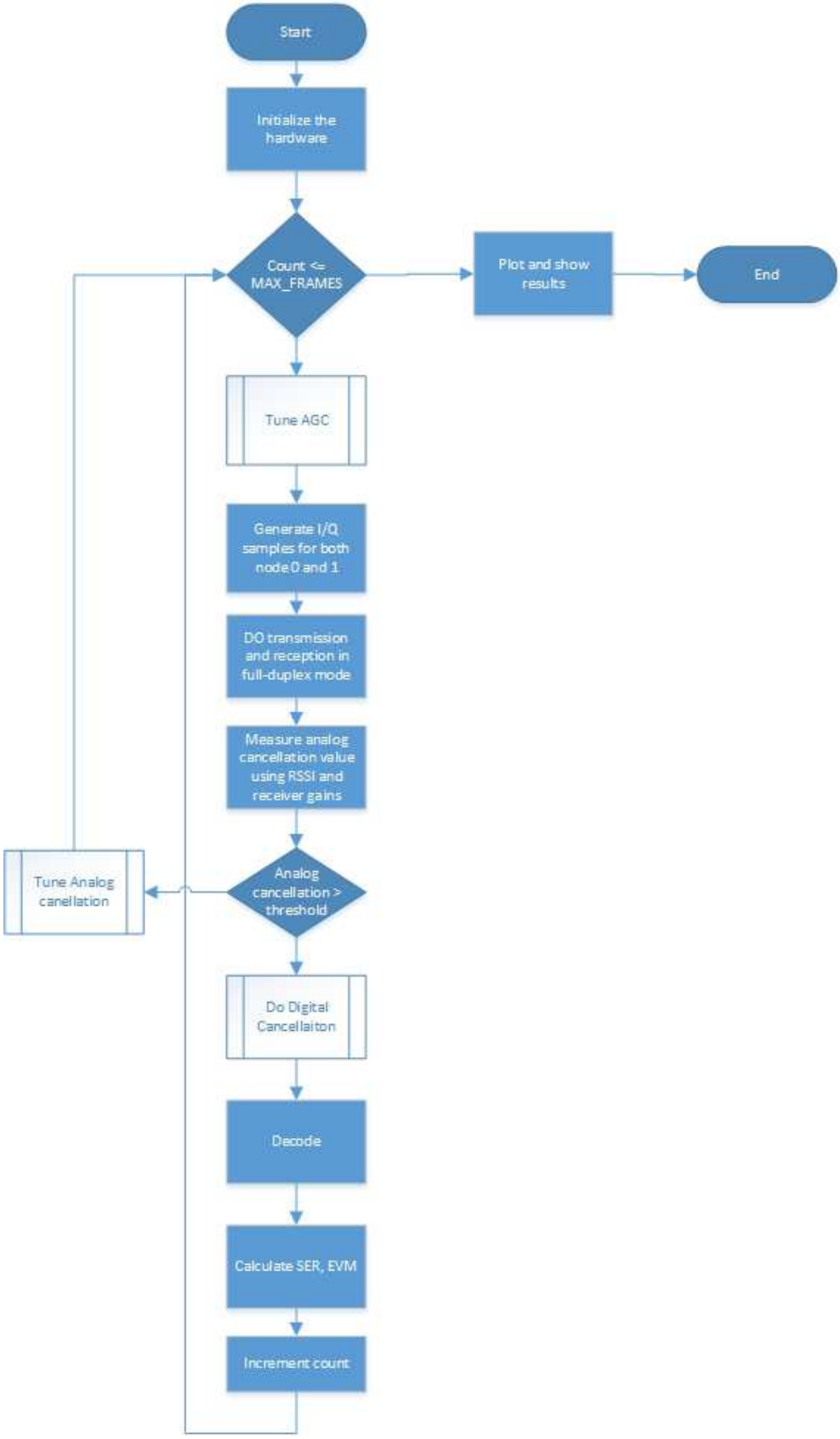


FIGURE 8. Data flow in the dual node setup.

As this setup deals with a link which includes a variable wireless channel whose coherence time is shorter than the complete transmission duration, thus, it is necessary to include an AGC implementation. The appropriate gain values for the receiver baseband and RF amplifiers are governed by the largest signal received. In order to ensure that no clipping at baseband happens, first required gain values are calculated for FD mode followed by HD mode. The smallest of these gain settings is used for doing the FD transmission. A predefined sequence consisting of four sinusoidal tones is sent from the transmitter in order to tune the AGC. AGC block is implemented in the FPGA [11].

In order to evaluate the performance of the wireless link, error vector magnitude (EVM) and symbol error rate (SER) metrics are calculated. EVM is calculated as follows

$$EVM_{dB} = 10\log_{10}\left(\left(\sum_{i=0}^{N}(I_i - \hat{I}_t)^2\right) + (Q_i - \hat{Q}_t)^2) / N\right) \quad (2)$$

Where I_i and Q_t are the i_{th} I and Q_t samples value of the transmitted signal, and $\hat{I}_i$ and $\hat{Q}_t$ are corresponding samples of the equalized received signal. N represents the number of complex symbols.

As already mentioned, this measurement setup is also used to demonstrate the adaptive nature of the analog cancellation solutions. With this regard, the analog cancellation stages are retuned when the analog self-interference cancellation excess a predefine threshold, i.e. 50 dB (the analog tuning is done in half-duplex mode). By doing so, the dual-node setup demonstrates a full-duplex wireless link while analog and digital blocks adapts to the time varying wireless channel.

3. VALIDATION OF THE ANALOG AND DIGITAL CANCELLATION BLOCKS

DUPLO demonstrator is integrated by different analog and digital solutions capable of cancelling the self-interference up to the receiver noise floor. The implementation, integration and validation of each key cancellation block are reported in this section.

3.1. ELECTRICAL BALANCE DUPLEXER

In WP2, two different electrical balance duplexer designs have been prototyped. D2.1 and D2.2 report on the design considerations and circuit performances gained both in simulations and in measurements. Different test setups have been used to measure the performance of the EBD. To maintain the timeline, only the first EDB design is considered in WP5, and the first validation results have been given in [1]. In this section, the validation of the EBD system in a single radio node configuration is continued. In section 4.1 two radio nodes will be considered (including a wireless communication link).

The test setup for the EBD system in a single radio node configuration is illustrated in FIGURE 9. A picture of this test setup is illustrated in FIGURE 3. It includes a Wireless open-Access Research radio Platform (WARP) version 3, the first version of the EBD RFIC CMOS chip-prototype [2] and a commercial planar inverted-F antenna (PIFA). WARPv3 integrates a high performance FPGA (Xilinx Virtex-6) and embeds two RF interfaces. Each RF interface can be configured to operate in transmission or in reception mode. The PC acts as the interface between WARPv3 and the EBD. The WARPLab v7.4 framework was used to perform data acquisition, while the main signal processing such as the tuning algorithm and calculating the SIC is performed on the PC.

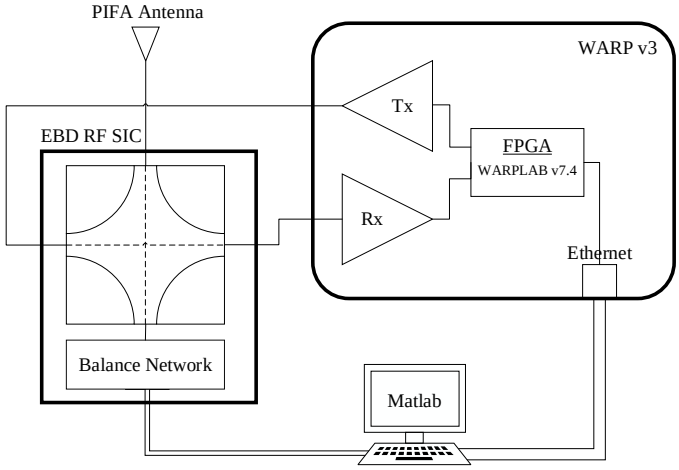


FIGURE 9. EBD system in a single radio node configuration.

In addition to the results presented in [1], different tuning algorithms have been developed. The tuning algorithms targets to tune the load of the balance network to match with the unknown and time-varying antenna impedance. Any mismatch results in a 'unbalanced' operation condition, degrading the SIC performance of the EBD. In an EBD, the SIC is quantified by the antenna impedance (Z_{ant}) and the balance network impedance (Z_{bal}), as follows:

$$SIC_{TX-RX}(dB) \propto -20\log_{10}(|\Gamma_{ant}(\omega) - \Gamma_{bal}(\omega)|) \quad (3)$$

where

$$\Gamma_{ant}(\omega) = \frac{Z_{ant}(\omega) - Z_o}{Z_{ant}(\omega) + Z_o} \tag{4}$$

and

$$\Gamma_{bal}(\omega) = \frac{Z_{bal}(\omega) - Z_o}{Z_{bal}(\omega) + Z_o} \tag{5}$$

In order to achieve the maximum SIC, $\Gamma_{bal}(\omega)$ should be balanced with $\Gamma_{ant}(\omega)$ across the channel bandwidth i.e. have the same frequency dependency. In the EBD RFIC used in this demonstrator, a balance network consisting of a variable R in parallel with a variable C was used. In order to achieve maximum SIC for this balance network, $|\Delta\Gamma| = |\Gamma_{ant}(\omega) - \Gamma_{bal}(\omega)|$ should be minimized across the channel bandwidth.

Two different tuning algorithms have been implemented. The first algorithm is based on a conventional binary search tree, and the second algorithm is more advanced and exploits specific characteristics of the EBD. Both algorithms have been developed to (a) maintain the normal transmit operation during tuning and to (b) preserve the digital design complexity.

(a) RF hardware tuning is generally a burden: it obstructs normal TX operation during tuning and it requires special training/test sequences which may be standard-incompliant. Both tuning algorithms target to overcome this burden by operating on the short training sequence (STS) which is part of every IEEE802.11 packet. While transmitting, the STS is used in the local node for SIC performance monitoring and to activate the impedance tuning when needed. In this way, the tuning can happen while preserving normal transmitter operation with only the receiver off (half-duplex mode). Once the required SIC is achieved, the transceiver can then restore its full FD capability.

In the IEEE802.11 standard, each STS consists of ten identical short symbols (800ns each). Each short symbol has the same frequency pattern which consists of 12 subcarriers distributed over the channel bandwidth. The characteristics of the STS are also useful for the SIC tuning algorithm as:

- Using specific frequency pattern allows enhanced detection in noisy ethers by using e.g. cross-correlation processing or averaging over consequent frequency responses.
- Using short symbols (800ns) allows for faster tuning compared to the longer training sequences.
- Using multiple identical symbols allows multiple tuning steps over the consequent symbols.

The only modification that would be required in the current standard to utilize the STS in the tuning algorithm, is increasing the number of symbols in the STS to satisfy the tuning algorithm requirements. Note that this overhead in the STS would be required only in the one packet at the tuning phase. For each tuning step, one symbol can be used to measure the SIC. After each measurement, processing is needed to calculate the next step which needs another one or more symbols according to the digital processing capability.

(b) Apart from the EBD, no dedicated analog circuitry or special antenna structures are required to enable FD operation. All signal processing, including monitoring and tuning, is performed digitally and can be implemented in the FPGA. Evidently, the tuning algorithm requires dedicated signal processing in digital baseband. To preserve the digital design complexity, the tuning algorithm can reuse the digital hardware resources of conventional OFDM-based TRX processors. The tuning algorithm for example, can sample the output of the RX FFT, and can thus reuse much of the RX digital hardware resources and functionalities.

Binary search tree

The binary search tree [14] is known as a simple and efficient method to reduce the search space in consequent iterative steps. During each iteration, maximally two measurements are performed (at the search edges). Based on these measured sample(s), the search space is halved for the next iteration. Given that the balance network consists of two tuning knobs, the R and C values are tuned consequently until the SIC exceeds the pre-defined threshold. A first version of the binary search tree has been discussed in [1]. An improved binary search tree has been implemented in the single-port antenna demonstrator presented in 4.1 in order to comply with the signal structure presented in section 3.3 and required for the digital cancellation.

EBD search algorithm

Equation (3) is exploited to develop an intelligent tuning algorithm which uses the measured SIC value to quantify the balance network impedance in order to reduce $|\Delta\Gamma|$ and improve the SIC. The usage of (3) allows the tuning algorithm to be parameterized for efficient tuning, and enables machine learning over multiple iterations [15].

The tuning algorithm is executed in two main phases. The first phase is the training and modeling phase during which the algorithm is trained to characterize the effect of digitally controlling the balance network on the SIC. By using data fitting techniques on the observed training points, a model of the circuit behavior is formed. This phase should be done once per chip after fabrication but should also be updated to improve the accuracy of the model across different operating conditions. During the second phase, the tuning is performed during system operation. The model first uses the measured SIC value to estimate $|\Delta\Gamma|$ based on (3). Then, a search algorithm identifies the actual phase of $\Delta\Gamma$. This second step is required as the SIC value is based on the magnitude $|\Delta\Gamma|$ only, but lacks the phase-angle information. After finding $|\Delta\Gamma|$, the model is used again to determine the required change in the R/C codes to minimize this difference.

Phase 1: The training and modelling phase gathers a data-set that describes the relation between the SIC and the R/C codes during constant antenna impedance conditions. As this data-set is gathered after fabrication, it includes the chip-to-chip process variations. Moreover, in order to increase the reliability of the modelling, the data-set can be updated during the TRX lifetime. Although this measurement requires constant antenna impedance conditions, it can be executed in a realistic environment since normal antenna impedance dynamic (tens of milliseconds) are slower than the whole training phase (tens of microseconds).

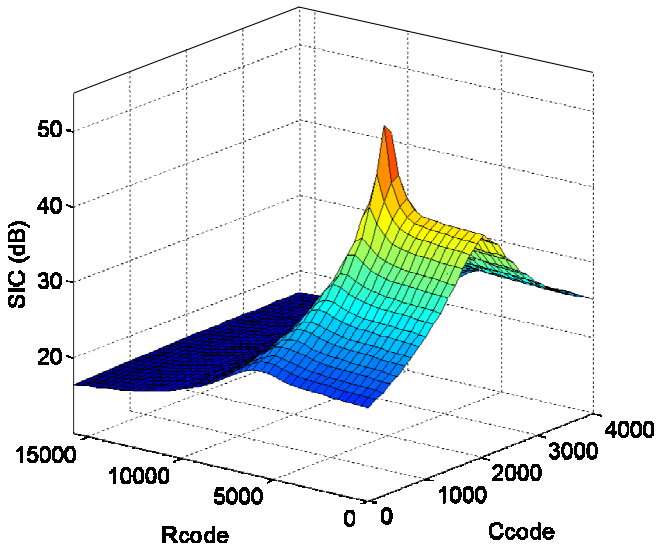


FIGURE 10. An example of the training data-set for the SIC versus resistance and capacitance codes

FIGURE 10 shows an example of the data-set gained from the training phase. The data-set covers the entire range of R/C codes. A coarse set of these codes can also be used in practice to minimize the measurement time, as long as the SIC surface pattern is sufficiently captured. Based on the obtained data-set, a mathematical model is derived by fitting the theoretical equations that describe the circuit.

The least squares method was used for data fitting, by using (3-5) in combination with the theoretical relationship between the R/C codes and the estimated balance network impedance:

$$C = C_{const} + k_{c1}C_{code}(0:3) + k_{c2}C_{code}(4:7) + k_{c3}C_{code}(8:11) \quad (6)$$

$$R = \begin{cases} R_{const} \,//\, k_r \,/(R_{code} * V_d - V_{th})\alpha, R_{code} < V_{th}/V_d \\ Rconst, Rcode \geq V_{th}/Vd \end{cases} \quad (7)$$

where R and C are the model values for the resistor and capacitor in the balance network impedance. R_{code} and C_{code} are the R/C codes of the resistance and the capacitance. C_{const}, k_{c1}, k_{c2}, k_{c3}, R_{const}, V_D, V_{th}, α and k_r are data fitting parameters derived from the theoretical equations describing the balance network impedance.

After fitting of the training data-set to the Equations (3-7), the model will include the best-fit values of Z_o and the parameters in (6,7) to provide:

- The relation between the measured SIC and $|\Delta\Gamma|$ (3).
- The relation between the modelled balance network impedances R and C versus the R/C codes (6,7) as shown in FIGURE 11.
- The relation between ΔΓ and the antenna impedance (4,5) where the balance network impedance is determined from (6,7) by using the current R/C codes.

By using this model and the measured SIC, the phase of $\Delta\Gamma$ is the only missing variable to calculate the R/C codes that balance the EBD and minimize the SIC.

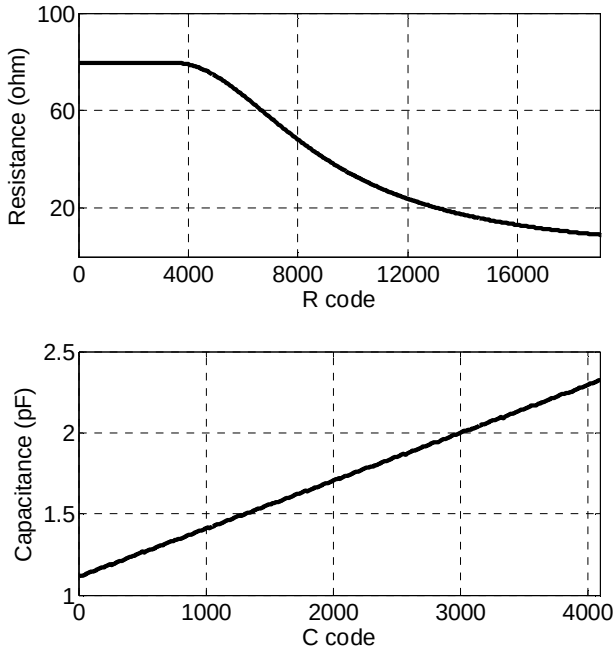


FIGURE 11. The model of the balance network resistance and capacitance versus R and C codes.

Phase 2: The angular search algorithm is applied during system operation. Then, the balance network is tuned by estimating $|\Delta\Gamma|$ from applying the measured SIC in the model derived in the previous phase. But as the antenna impedance is a complex value, the magnitude value $|\Delta\Gamma|$ only is not sufficient for proper quantification. Therefore, an angular search algorithm is required to determine also the phase of $\Delta\Gamma$ to be able to use the model to find the required R/C codes.

This technique relies on changing the phase of $\Delta\Gamma$ while maintaining its magnitude (determined by the measured SIC). Using the model again, the system can determine the change in the corresponding R/C codes needed to test this specific phase as shown previously using (3-7). By applying these R/C codes and measuring the corresponding SIC, the search algorithm can find the optimum phase. As an illustration of this process, FIGURE 12 shows the measured SIC in function of phase-rotating the balance network impedance. Over 360 degrees phase rotation, the SIC shows a bell-shape behaviour only one maximum and one minimum. FIGURE 12 shows an important property in the curve where any phase near the maximum SIC will always have higher SIC than further phase. This shape enables the usage of efficient search techniques to determine the optimum phase towards which the balance network impedance needs to be tuned.

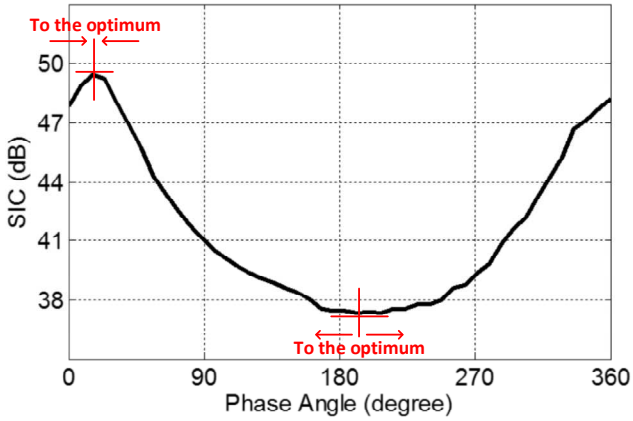


FIGURE 12. An example of the measured relation of SIC with the phase angle of $\Delta\Gamma$ showing the two paths from the minimum SIC to the maximum SIC.

The angular search starts as illustrated in FIGURE 13, when the system measures the SIC in its current situation (point "0") below its determined threshold. Next, the system measures three SIC measurements of which the angle of $\Delta\Gamma$ is 120 degrees spaced as illustrated with a point "1". Based on the SIC values in these three points, the algorithm will limit its search between the two angles with highest SIC; For example, if the highest SIC were at 120° and 240° phase angle, the search algorithm then will continue by testing the angle in middle (180° phase angle). This process then repeats until the optimum angular phase is found. Note however that the points on FIGURE 13 are not ideally circular, although the $|\Delta\Gamma|$ magnitude remains constant. That is because the relation is not linear between the digital R/C codes and the effective reflection coefficient values.

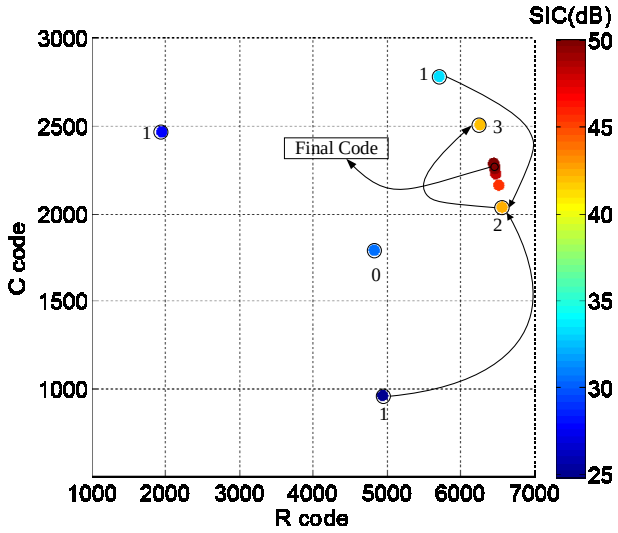


FIGURE 13. An example of the development of the angular search.

The EBD search algorithm has been experimentally validated in a single radio-node setup, comprising an EBD RFIC, WARPv3 with WARPLab (IEEE802.11 channels with 20MHz bandwidth, operating in the 2.4GHz ISM band) and a WiFi PIFA antenna. Different environmental scenarios were tested (e.g. antenna movement, placing nearby metal objects, hand movement, etc.). These different scenarios impact the antenna impendence and cause imbalance with the impedance of the (un-tuned) balance network which will degrade the SIC as illustrated in FIGURE 14 at tuning step (0). After starting, the tuning algorithm steps towards an improved SIC for each different scenario; FIGURE 14 indicates that the required SIC values are achieved after about 10 tuning steps. Given this low amount of tuning steps, efficient and rapid re-tuning with minimum overhead on the communication operation is enabled. It can be observed that this tuning algorithm provides an average RF-SIC across the 20MHz wide channel up to 50dB.

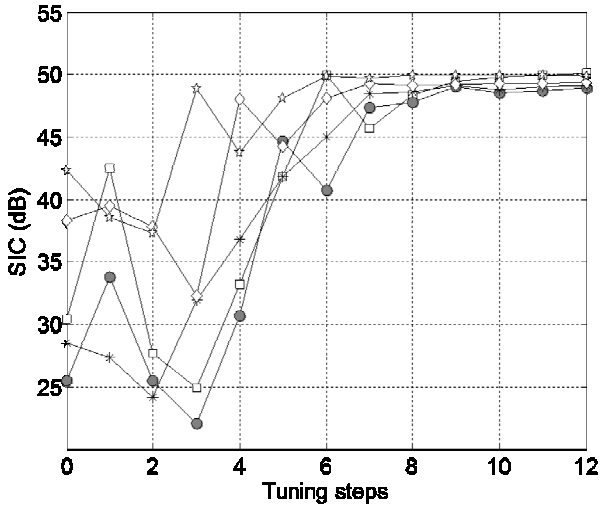


FIGURE 14. The RF-SIC during the tuning algorithm operation in different environmental variations.

3.2. DUAL-POLARIZED ANTENNA AND ACTIVE CANCELLATION NETWORK

This section describes the validation of the dual-polarized antenna and the active cancellation network. Additionally, the implementation and integration of the prototypes integrated in the dual-port antenna demonstrator are also described in this section.

3.2.1. Dual-polarized microstrip antenna

The antenna solution integrated in the dual-port antenna demonstrator consists of a single antenna solution which makes use of the antenna polarization to prevent self-interference. The antenna has two feeding ports which excite linear vertical and horizontal polarizations. With the aim of suppressing the cross-polarization at each excitation port, and thus improving the isolation, the antenna structure consists of a microstrip stacked-patch structure with a pair of coupling slots excited by means of a symmetric 180º phase shift network. The first prototype of this dual-polarized antenna was reported in [2] and [1], while [3] describes the design and implementation of the second antenna prototype which provides improvements in terms of size and operational bandwidth. FIGURE 15 shows the second prototype of the dual-polarized antenna which has been used for the integration in the final demonstrator.

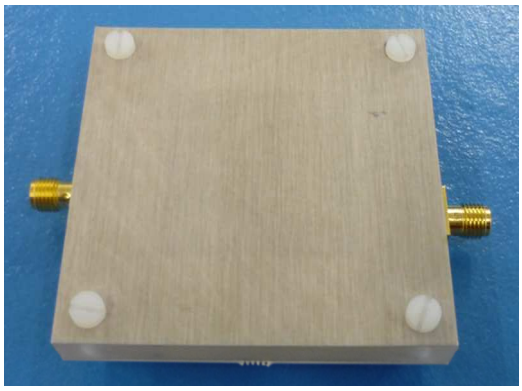


FIGURE 15. Dual-polarized antenna prototype integrated in the demonstrator.

The second prototype of the dual-polarized antenna includes an improved excitation network and a dielectric layer between excitation and radiation patches, in order to improve the matching bandwidth maintaining the self-interference suppression level of 50 dB.

This second prototype of the dual-polarized antenna can operate over the signal bandwidth defined for the DUPLO proof-of-concept, however, the improvements included in this new antenna model allows the antenna to operate over wider bandwidths as the WiFi band (2.4-2.48 GHz), as TABLE 1 depicts.

TABLE 1. Summary of technical specifications for the second dual-polarized antenna prototype.

DUPLO demonstrator BW = 20 MHz	WiFi band 2.4 - 2.48 GHz
Antenna Size: 60 x 60 x 8 mm Dual linear polarized antenna : V/H polarization RF interface : SMA connector	
Antenna Return loss < -14 dB	Antenna Return loss < -9 dB
Antenna Isolation < -49 dB	Antenna Isolation < - 42 dB
Antenna Gain > 6.3 dB	Antenna Gain > 5.5 dB
Antenna XPD > 23 dB	Antenna XPD > 20 dB
3dB BeamWidth > 70º	3 dB BeamWidth > 75º
Antenna efficiency > 74%	Antenna efficiency > 70%

The self-interference suppression provided by the dual-polarized antenna has been measured using the integration platform, i.e. the WARP platform. In doing so, a 20 MHz 16-QAM digital modulated signal centered at 2.457 GHz was generated with WARP board, and the spectrum of the self-interference after the dual polarized antenna was measured. FIGURE 16 shows how the self-interference is 50 dB below the transmitted signal in the overall antenna bandwidth.

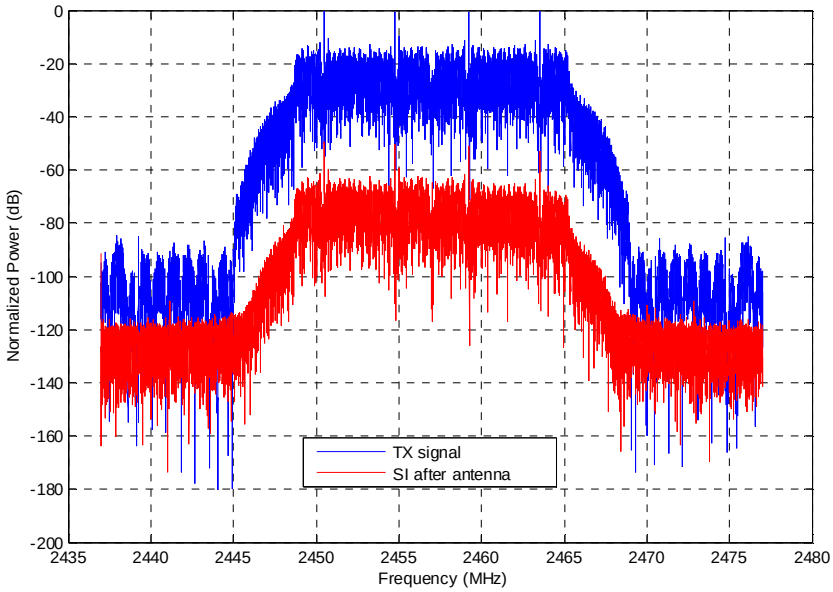
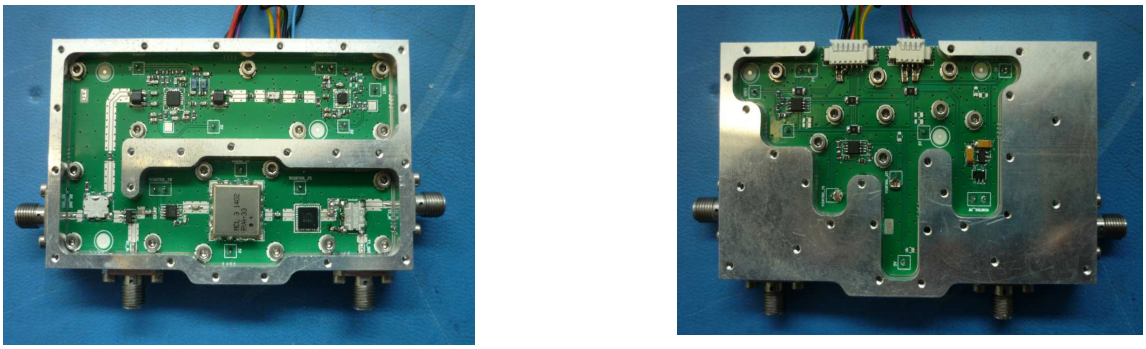


FIGURE 16. Spectrum of the SI after the dual-polarized antenna.

3.2.2. Active cancellation network

The self-interference suppression achieved at antenna level is really sensitive to the changes in the environment close to the full-duplex transceiver. Nearby objects close to the antenna can degrade the self-interference suppression achieved at antenna level in more than 10 dB as demonstrated in deliverable D2.1 [2]. However, if the digital cancellation cannot compensate this degradation, the signal-to-noise ratio of the overall receiver will be reduced. With the aim of maintaining a good level (>50dB) of self-interference cancellation before the LNA, the dual-polarized antenna has been combined with an active cancellation network which operates on RF signals. This active cancellation network consists of a tunable cancellation network capable of adapting dynamically to the changes of the self-interference channel, as previously reported in deliverables D2.2 [2] and D5.1 [1]. The cancellation network uses an attenuated and phase shifted copy of the transmitted RF signal to cancel the self-interference that leaks from the dual-polarized antenna.

The active cancellation network has been implemented in an integrated PCB using off-the-shelf components. The first developed prototype, reported in the deliverable D5.1 [1], used a vector modulator to implement the variable attenuation and phase shift. However, some limitations in terms of amplitude/phase resolution were founded with this prototype, reducing the number of scenarios over which the active cancellation can recreate the inverse of the self-interference signal. Due to this reason, a new active cancellation prototype was designed and implemented as deliverable D2.2 [2] describes. This new active cancellation board implements the variable attenuation and phase shift by means of using analog controlled attenuator and phase shifter. With this new design, a fine-grained control of the attenuation and phase shift coefficient is achieved, which allows to cover a wide range of scenarios. FIGURE 17(A) and FIGURE 17(B) show the top and bottom layers of the manufactured PCB. The description of the architecture and the discrete components employed in the implementation of the active cancellation network has been included in the deliverable D2.2 [2], as well as the electrical specifications of these components.



(A) (B)

FIGURE 17. Active cancellation new board. (A) Top, (B) bottom.

The active cancellation network incorporates a logarithmic power detector that acts as a receiver SI signal strength indication (RSSI). By doing so, the power detector monitories the received SI signal power after cancellation, which is used to automatically adjust the phase and attenuation coefficients by means of implementing a gradient descent algorithm as deliverables D5.1 [1] and D2.2 [2] describe. This automatic tuning algorithm minimizes the power of the self-interference by adjusting the settings of the attenuator and phase shifter in response to the wireless channel changes. The STM32F4 [16] microcontroller is used to control the settings of the active cancellation network. This microcontroller also runs the automatic tuning algorithm.

As described in deliverables D2.1 [2] and D2.2 [3] the main limitation of the active cancellation network is its limited cancellation bandwidth. As D2.2 describes, the self-interference signal after the dual-polarized antenna presents a group delay which can reduce the cancellation bandwidth if this group delay is not applied to mimic the self-interference. With the aim of analyzing the benefits of including a variable delay line in the active cancellation network, a new board has been implemented including three integrated delay lines and digitally controlled switches to adapt the group delay from 2.2 ns to 6.6 ns, as deliverable D2.2 [3] describes. FIGURE 18 shows the active cancellation board with the delay line and the dual-polarized antenna.

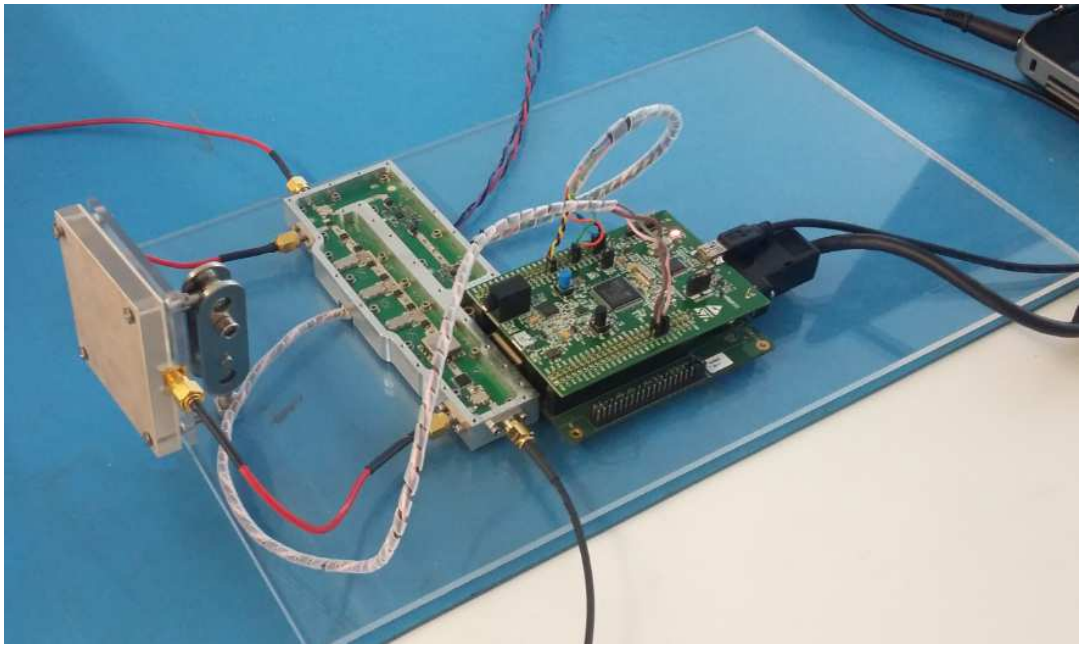


FIGURE 18. Active cancellation network with delay line integrated with the dual-polarized antenna.

The cancellation provided by this new board was measured and the results are shown in FIGURE 19. This figure shows the self-interference cancellation over frequency for three different group delays, i.e. when the group delay is zero, when the group delay is 2.2 ns (delay 1) and when the group delay is 4.4 ns (delay 2). As can be seen from the obtained results, the longer the group delay the wider cancellation bandwidth (for group delays longer than 4.4 ns, a reduction of the cancellation BW was observed). If 60 dB of SIC is considered as the target SIC, the cancellation bandwidth is practically doubled when a delay line of 4.4 ns is applied in the active cancellation network.

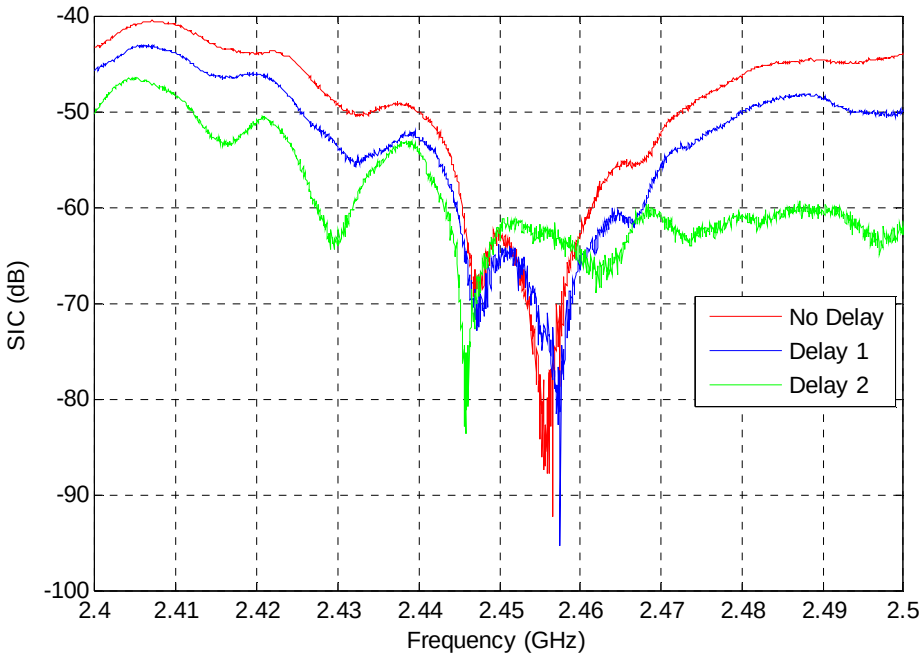


FIGURE 19. Self-interference cancellation provided by the active cancellation network with a variable delay line.

According to these results, analog delay lines increase the self-interference cancellation performance of the full-duplex transceiver in terms of SIC bandwidth. However, they increase the size of the analog circuits. Moreover, the automatic tuning of these new solutions requires more complexity as they increase the number of unknowns in the tuning algorithms. This issue needs to be addressed and further investigation is required in the future. Due to these reasons, the active cancellation network without the delay line is used for integration in the DUPLO demonstrator.

3.2.3. Dual-polarized antenna and active cancellation integration

The dual-polarized antenna has been integrated together with the active cancellation network and the WARP platform. The main interfaces among these key building blocks were defined in the deliverable D2.2 [2], however these interfaces have suffered some minor modifications. As can be seen from FIGURE 20, the WARP board is connected to the control PC via Ethernet. Additionally, the gradient descent algorithm has been implemented in the microcontroller, and it is activated from the control PC via the serial port. Initially, the analog tuning algorithm would be activated from the WARP FPGA via three level signals and a level shifter, however, the changes in the demonstrator framework entailed the analog tuning activation from the control PC. This new configuration allows the tuning activation in an efficient way via the RS232 line. By doing so, one activation command is sent from the PC to the microcontroller when the analog SIC is below a predefined threshold, i.e. 50 dB. Then STM32F4 runs the gradient descent algorithm and sets the analog control voltages of the attenuator and phase shifter which minimize the power of the self-interference signal after analog cancellation. Moreover, external power supply (+5V and +10.8V) is used to power the active cancellation

network. TABLE 2 lists the interfaces used to connect and control the active cancellation network with the rest of the building blocks.

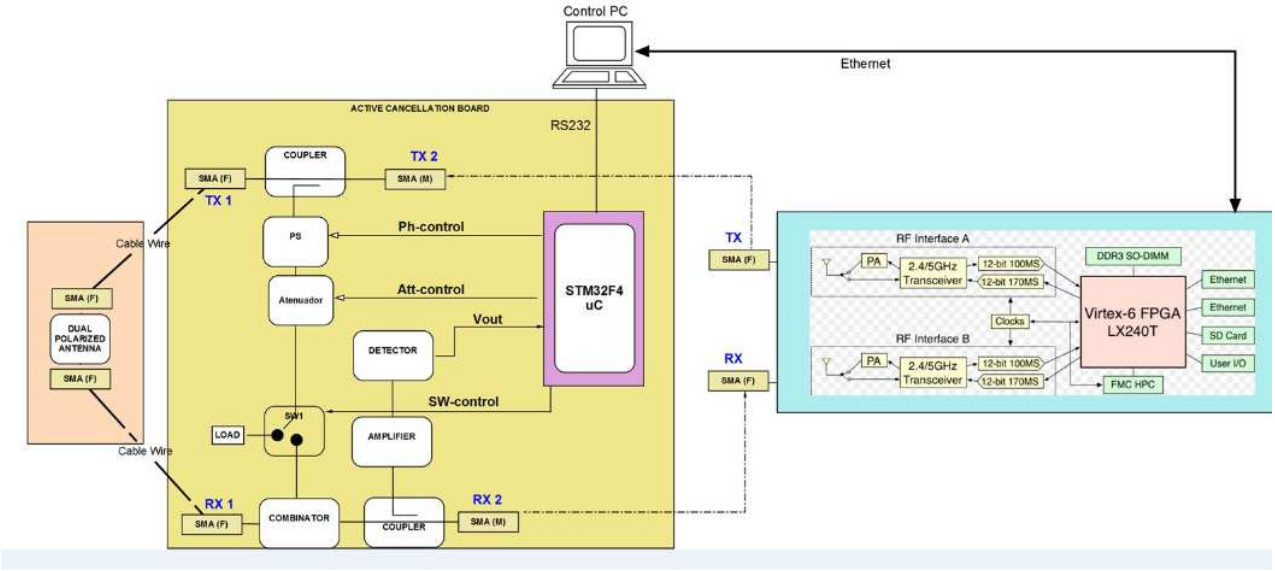


FIGURE 20. Dual-polarized antenna and active cancellation integration within DUPLO demonstrator.

TABLE 2. Description of the interfaces defined for dual-polarized antenna and active cancellation network integration.

Interface	Signal description
Ph-control	Analog signal to control variable phase shifter
Att-control	Analog signal to control variable attenuator
SW_control	Digital signal to enable /disable cancellation branch.
Vout	Analog signal to monitor the SI RSSI
TX,TX1,RX1,RX2	SMA connector for RF signals connection from/to antenna and from/to WARP. RF signal at 2.45GHz

The gradient descent algorithm works in steps, and at each iteration it computes the slope of the self-interference power by changing the attenuation and phase shift a predefine step size, as [3] describes. The STM32F4 microcontroller uses two 12-bits DAC to set the analog control voltages of the attenuator and phase shifter. Additionally, the active cancellation network has two operational amplifiers to convert the output voltage of the microcontroller (0-3V) to the adequate analog voltage range of the attenuator (0-5V) and phase shifter (0-9V) respectively. Furthermore, the analog signal generated by the power detector is digitalized by the microcontroller by means of using a 12-bit ACD.

As already mentioned, the current demonstrator is based on the WARPLab v7.4 framework. This allows to generate the I/Q signal samples in MATLAB and send them to WARP through the Ethernet cable. Then the

samples are up-converted to the desired frequency and transmitted to the active cancellation network TX port. Likewise, the received signals at WARP RX port are down-converted and the I/Q signal samples are also sent to the control PC via the Ethernet line. The WARP radio board transmits/receives the RF signals to/from the active cancellation network by means of using SMA connectors and short-length RF cables, in order to reduce the insertion losses in the transmission and reception paths (< 0.5 dB in the TX chain and < 1 dB in the RX chain). Similar configuration is used to connect the dual-polarized antenna and the active cancellation network. Moreover, an antenna support is also used in order to orientate the dual-polarized antenna to the desired pointing direction as can be seen in FIGURE 21.

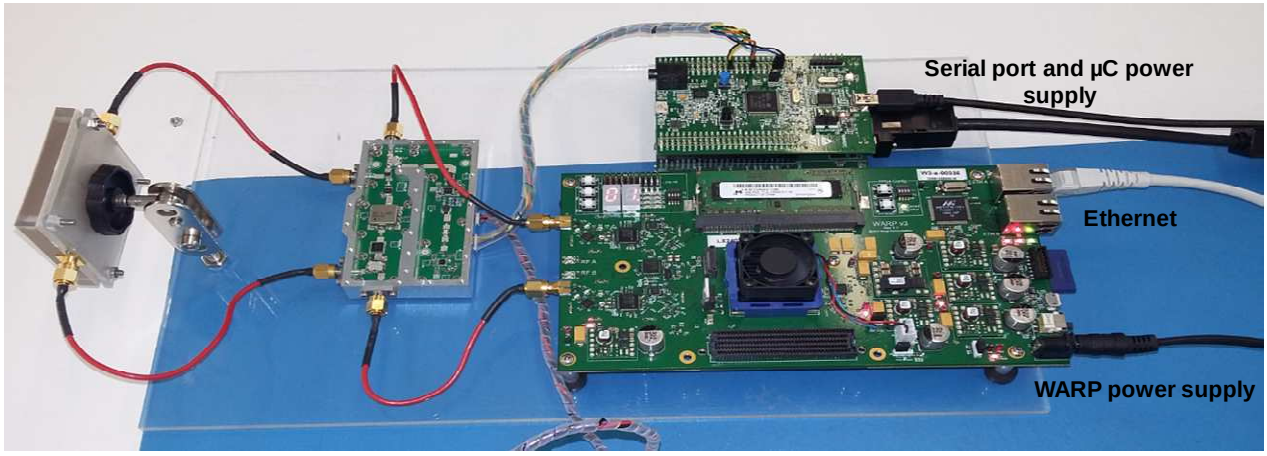


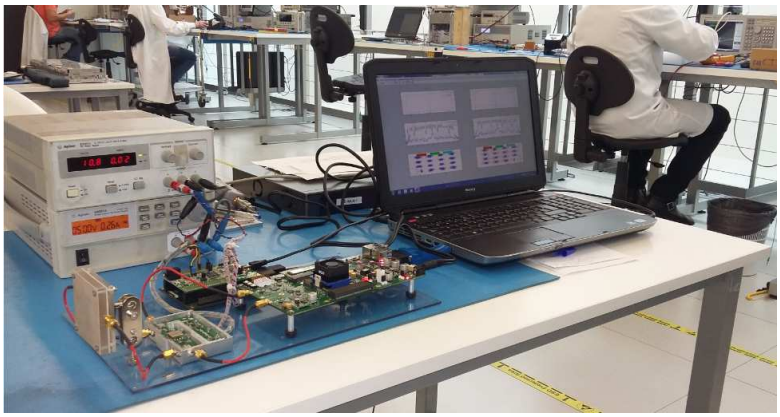
FIGURE 21. Integration of the dual-polarized antenna and the active cancellation network.

3.2.4. Dual-polarized antenna and active cancellation validation

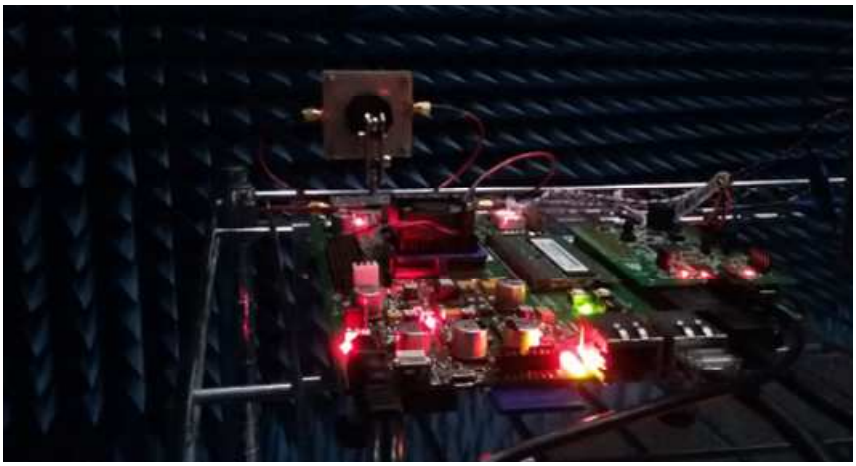
In this section it is presented the results of the experimental validation of the cancellation capabilities of the dual-polarized antenna and the active cancellation network. For that purpose, we have validated the SIC performance for different transmit powers and signals across the following scenarios:

- Moderate multipath scenario: the full-duplex node has been placed inside a radiofrequency laboratory with RF equipment working and people moving around it.
- No-multipath scenario: the full-duplex node has been placed inside an anechoic chamber where neither reflections form the environment nor interference signals occur. The only possible reflections come from the own full-duplex radio node or its support.
- Strong-multipath scenario: two metallic objects where placed close to the dual-polarized antenna at a maximum distance of 80 cm.

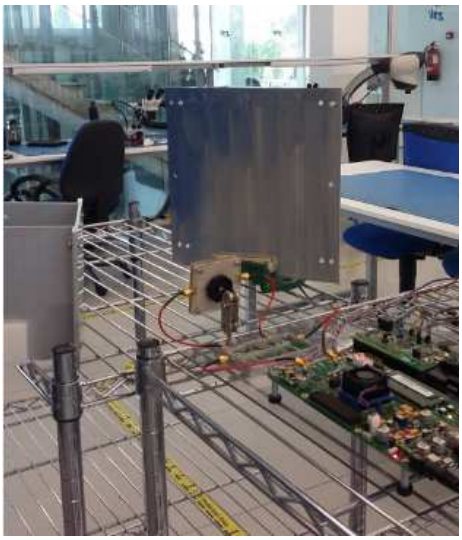
FIGURE 22 shows pictures of the dual-port antenna demonstrator in the three different abovementioned scenarios.



(A)



(B)



(C)

FIGURE 22. Evaluation of the cancellation capabilities of the dual-polarized antenna and the active cancellation network under different scenarios. (A) Moderate multipath scenario, (B) no-multipath scenario and (C) strong-multipath scenario.

For each scenario, the transmit signal has been generated using the WARPLab v7.4 framework and WARP radio board. A 20 MHz BPSK digital modulated signal was generated using different transmit powers from 0dBm to 20 dBm (this transmit power corresponds to the PTX measured at the WARP output). For each scenario and PTX, it has been conducted 30 runs of the gradient descent algorithm and it has been computed the average analog self-interference across those runs. FIGURE 23 shows the analog self-interference for different transmit powers when the dual-port antenna demonstrator is placed in the moderate multipath scenario. As can be seen from the obtained results, the active cancellation network improves in around 10 dB the self-interference isolation provided by the antenna, achieving an analog SIC of 60 dB in 20 MHz BW for a variety of transmit powers up to an including the maximum PTX of 20 dBm.

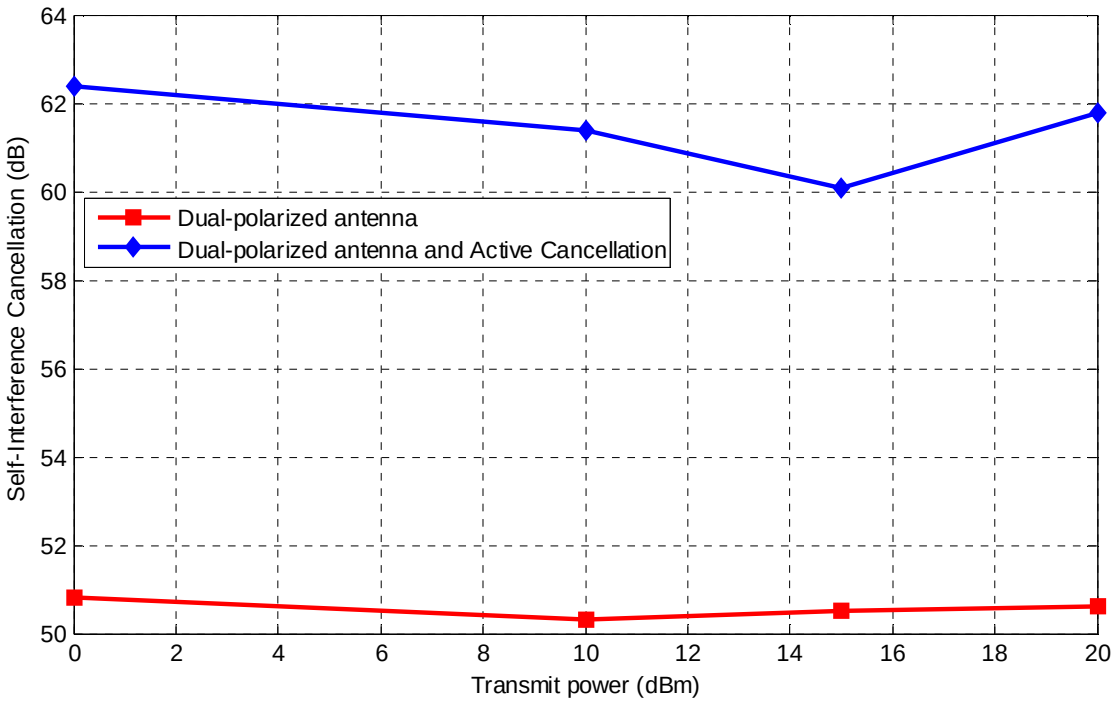


FIGURE 23. Analog SIC of dual-port antenna demonstrator for different transmit powers and 20 MHz signal BW (moderate multipath scenario).

FIGURE 24 plots the cumulative distribution function (CDF) of the analog SIC for two different signal bandwidths, i.e. 20 MHz BW and 10 MHz BW. As can be seen from the obtained results, the loss in the analog SIC is less than 2 dB when the wider BW is considered.

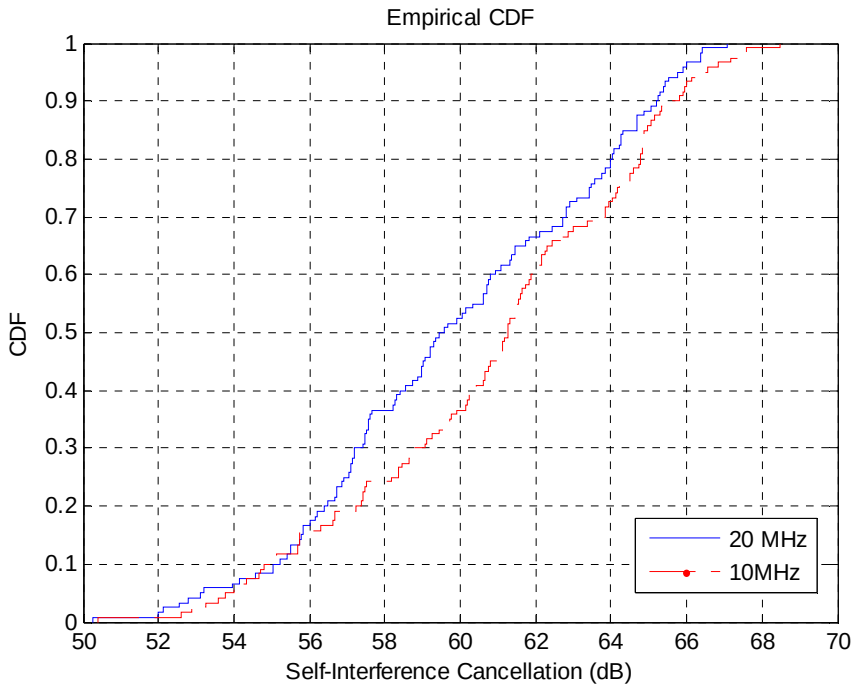


FIGURE 24. CDF of analog SIC with changing signal bandwidths.

As already mentioned, it has been conducted several analog cancellation tunings to adapt the attenuation and phase shift coefficients to the self-interference channel by means of running the gradient descent algorithm in the STM32F4 microcontroller. This gradient descent algorithm takes approximately between 12-15 steps to converge. In terms of time, the gradient descent algorithm takes approximately 12 milliseconds (median value) to converge to the required self-interference cancellation value, as FIGURE 25 illustrates. This tuning time could be reduced if the tuning algorithm is implemented in the FPGA.

During the period of time required for the tuning algorithm to converge, the full-duplex radio node works in half-duplex mode and only the tuning signal is transmitted. The performance of the tuning algorithm is independent on the tuning signal and the same performance in terms of convergence time and SIC is achieved when continuous or standard OFDM signals are used, as FIGURE 26(A) and FIGURE 26(B) illustrate. Furthermore, the active cancellation has to be re-tuned when there is a change in the environment close to the dual-polarized antenna. The frequency to do the re-tuning depends on the environment, for instance indoor environments are usually very dynamic and the changes in the environment are frequent, however outdoor scenarios would be easier since changes in the near field occur less frequently. With the aim of reducing the overhead due to analog tuning, an analog SIC threshold of 50 dB has been defined. This way, the active cancellation is only re-tuned when the analog SIC drops below this threshold.

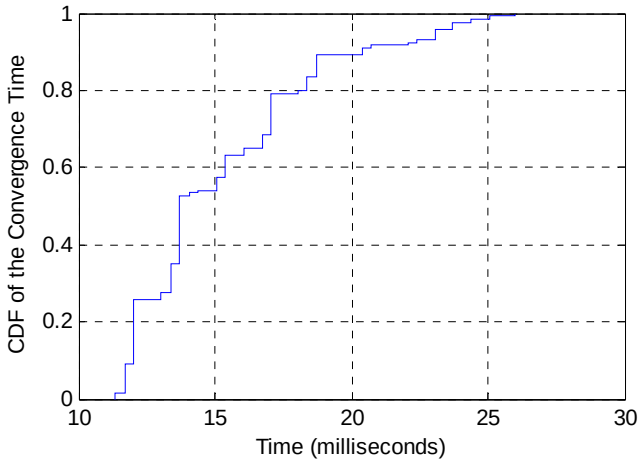
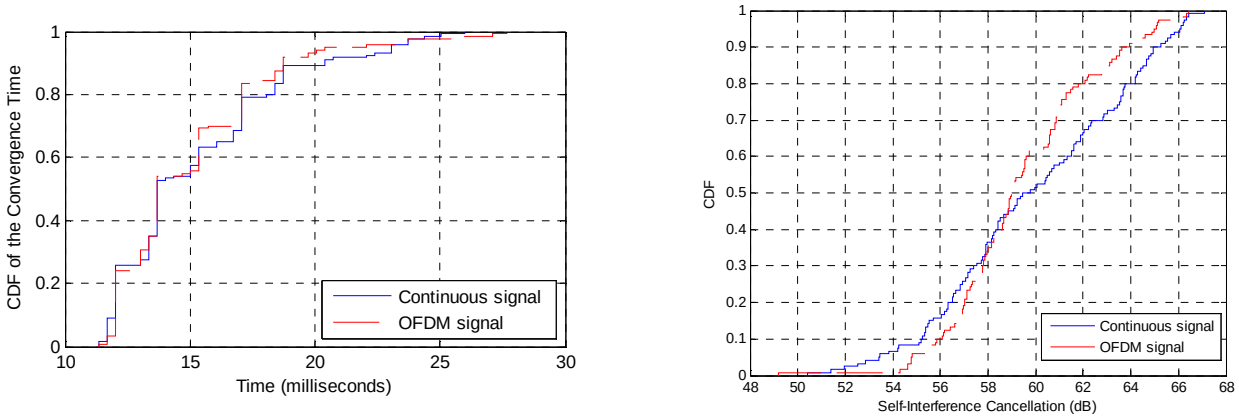


FIGURE 25. CDF of the convergence time for the gradient descent algorithm.



(A) (B)

FIGURE 26. (A) CDF of the convergence time for different tuning signals, (B) CDF of the analog SIC for different tuning signals.

FIGURE 27 shows the performance of the dual-polarized antenna and the active cancellation in different scenarios. As can be seen from the obtained results, there is a maximum degradation of the self-interference suppression provided by the dual-polarized antenna of almost 8 dB when the metallic objects are placed close to the antenna (compared with the scenario with moderate multipath). However, the active cancellation increases the isolation from the antenna, maintaining the analog SIC above 50 dB, even in the worst case scenario (the one with metallic objects). Moreover, the digital cancellation also counteracts the loss in analog SIC, reducing the remaining self-interference up to the receiver noise floor as will be shown later in this document.

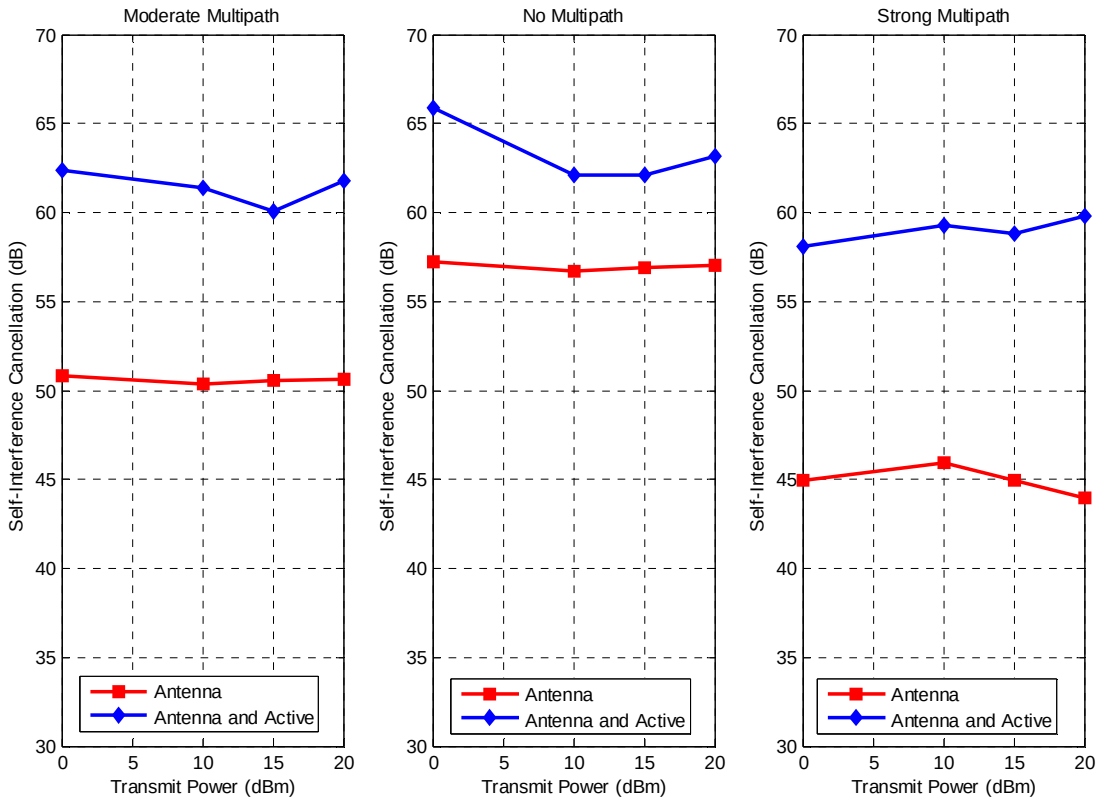


FIGURE 27. (A) Dual-polarized antenna and active cancellation performance for different scenarios.

3.3. FULL-DUPLEX BASEBAND

An OFDM based waveform is utilized in the demonstrator. In total, it consists of sixty four subcarriers out of which fifty two are used as data carriers and pilots. To mitigate the inter symbol interference caused by the multi-path wireless channel, sixteen sample cyclic prefix is prepended with the waveform. FIGURE 28 shows the transmitted frame structure in time domain for the two node link setup, i.e. two full-duplex nodes separated a certain distance operating both in FD mode. The long training sequence (LTS) is used for detecting the symbol boundary and calculating the frequency offset. The short training sequence (STS) purpose is to train the automatic gain controller (AGC) [11]. As the receiver gains are being set to a fixed value during the transmission of a frame, the STS part is not required. However, in the demonstrator is still being transmitted. The STS, LTS and Training sequence is collectively referred as the preamble in this document. For Node 0 transmission, zeros are inserted in between the preamble and the data part. The number of zero samples is denoted by D, whose value is equal to the length of the preamble and a fixed delay of 200. One sample delay is equal to 25ns because the sampling frequency is equal to 40 MHz. In case of Node 1, zeros are transmitted first followed by preamble and data. The zeros are used to transmit the preambles in a time orthogonal manner. In case of the single node setup, the frame is almost similar to the dual node case except that no zeros are added to the transmission.

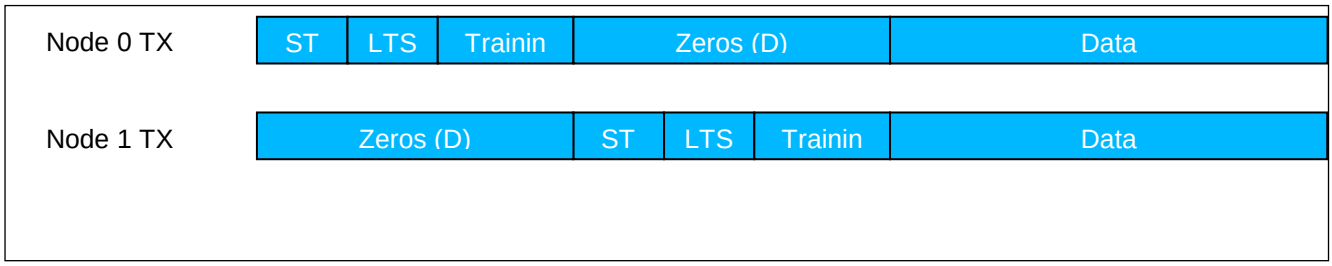


FIGURE 28. Time domain representation of the full-duplex frame.

FIGURE 29 shows the frame structure in the frequency domain. There are four data sub-carriers reserved for pilots for each node i.e., in total eight pilot tones are used while operating in full-duplex mode. Pilots are used to correct the residual phase in each OFDM symbol. Pilots for node 0 and node 1 are orthogonal in frequency domain. When doing transmission in half-duplex mode, the same number of data carriers and pilots are used as in full-duplex case i.e., the extra 4 pilots are set to zero when doing half-duplex transmission.

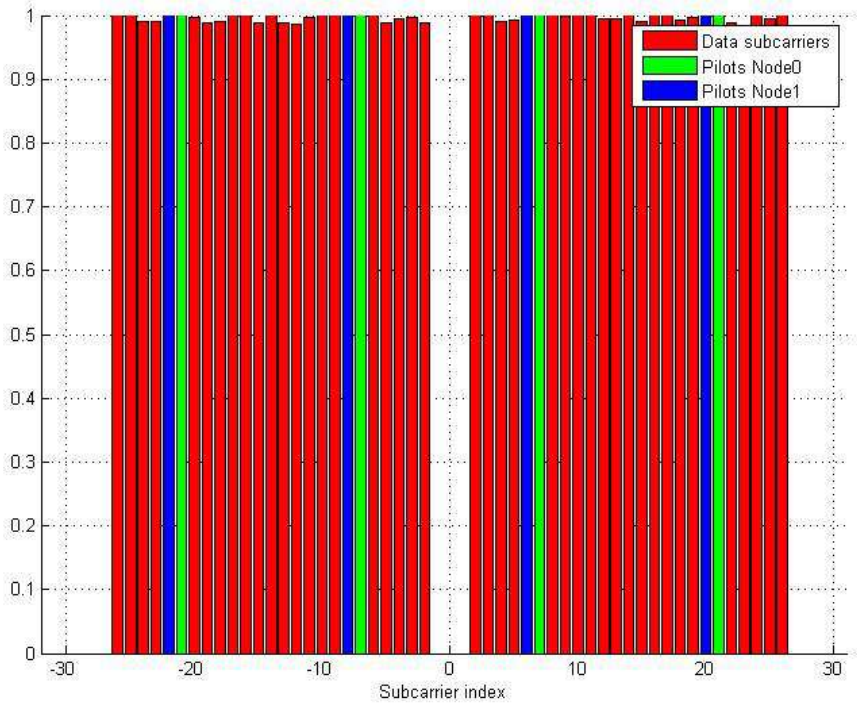


FIGURE 29. OFDM symbol in frequency domain.

In order to decode the received data and to do self-interference cancellation, an estimate of the channel is needed. The training sequence is used for calculating the channel estimate. It consists of two OFDM symbols, each sub-carrier of which is modulated with a pseudo random BPSK symbol. The training symbol differs from the normal OFDM symbol in the sense that it has a DC component and its bandwidth is larger than the normal OFDM symbol. This modification helps in the case of time domain cancellation of the self-interference. FIGURE 30 shows the spectrum of the residual SI signal after doing digital cancellation in time domain. The original training sequence refers to a training sequence which has no DC component and its bandwidth is equal to the data OFDM symbols. The modified training sequence refers to the sequence which has a DC component and which spans the whole transmission bandwidth. It can be seen that the modified sequence improves the cancellation close to the DC and the corner sub-carriers.

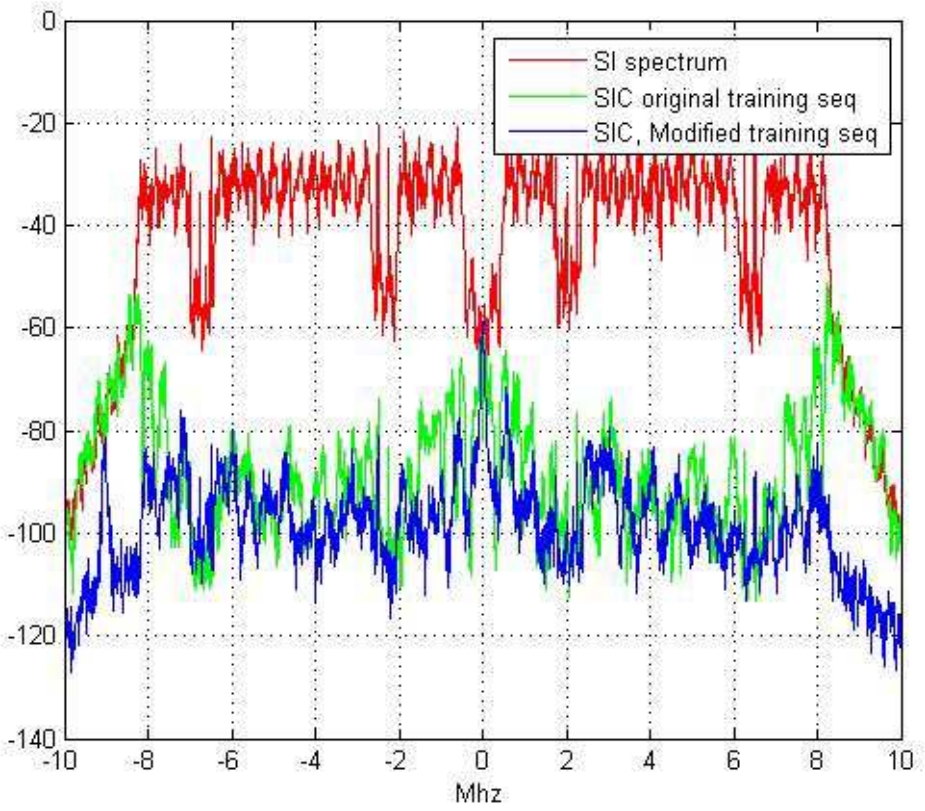


FIGURE 30. Time domain SIC performance comparison for different training sequences.

As each subcarrier is independent of each other, an estimate of each sub-carrier is calculated using a least-square estimate.

$$\hat{h}_k = \frac{T_k^* * (r_{1,k} + r_{2,k})}{2} \tag{8}$$

for the k_{th} sub-carrier, $\hat{h}_k$ represents the estimate, T_k^* is the conjugate of the transmitted training symbol and $r_{1,k}$ and $r_{2,k}$ represent the received symbol on the first and second training symbol. Equalization is performed in the frequency domain by zero-forcing i.e., the estimate of the transmitted symbol $\hat{x}_k$ is calculated as

$$\hat{x}_k = r_k / \hat{h}_k \tag{9}$$

As the clocks used by the two WARP boards are not phase locked with each other, there is a continuous phase shift in the received OFDM symbol. To mitigate the rotation of the received constellation, the pilot sub-carriers are used to calculate the required phase rotation, afterwards this phase rotation is applied to each received OFDM symbol. The average phase shift for each OFDM symbol is calculated as,

$$\partial\theta = (\partial\theta 1 + \partial\theta 2 + \partial\theta 3 + \partial\theta 4)/4 \tag{10}$$

where $\partial\theta_i$ is the phase difference between the phase of the received and the transmitted i_{th} pilot.

3.3.1. DIGITAL CANCELLATION BLOCK

Digital cancellation block forms a part of the digital baseband. Digital cancellation is implemented as a feed forward filter. Considering a linear system model in time domain,

$$y_t = h_{t,SI} * x_{t,SI} + h_{t,Des} * x_{t,Des} + n \tag{11}$$

Where $h_{t,SI}$ and $h_{t,Des}$ are the self-interference and desired channel respectively, $x_{t,SI}$ and $x_{t,Des}$ represents the transmitted self-interference and desired symbols, $(*)$ represents the convolution operation and n represents the noise. The previous equation can be written in frequency domain as,

$$y_f = h_{f,SI} * x_{f,SI} + h_{f,Des} * x_{f,Des} + n_f \tag{12}$$

Based on the models represented in Equations (11) and (12), digital cancellation can be defined as

$$SIC_{t,D} = y_t - \hat{h}_{t,SI} * x_{t,SI} \tag{13}$$

$$SIC_{f,D} = y_f - \hat{h}_{f,SI} * x_{f,SI} \tag{14}$$

Furthermore, as OFDM is used as the modulation technique, each sub-carrier can be treated independently in the frequency domain, thus leading to a sub-carrier based cancellation

$$SIC_{k,f,D} = y_{k,f} - \hat{h}_{k,f,SI} x_{k,f,SI} \tag{15}$$

These linear models lead to two different implementations of digital cancellation, which are

- Time domain cancellation,
- Frequency domain cancellation.

When the SI cancellation is performed using Equation (13), then it is referred as time domain cancellation. Similarly, cancellation performed using Equation (15), is referred as frequency domain cancellation. The selection criterion depends upon the symbol boundary. The symbol boundaries in the received signal are derived from the LTS sequence. Due to propagation delay and trigger delay, there can be a mismatch between the symbol boundaries of the two nodes in the received signal. FIGURE 31 shows the distribution of the difference between the sample boundary of self-interference and desired signal. Since OFDM can only be demodulated at the correct symbol boundary, this makes it necessary to include implementations of both frequency domain and time domain interference cancellation algorithms in the demonstrator. In case the symbol boundary is same for the SI and desired signal, i.e., the difference between the symbol boundaries is zero, then frequency domain cancellation is used, otherwise, time domain cancellation is used.

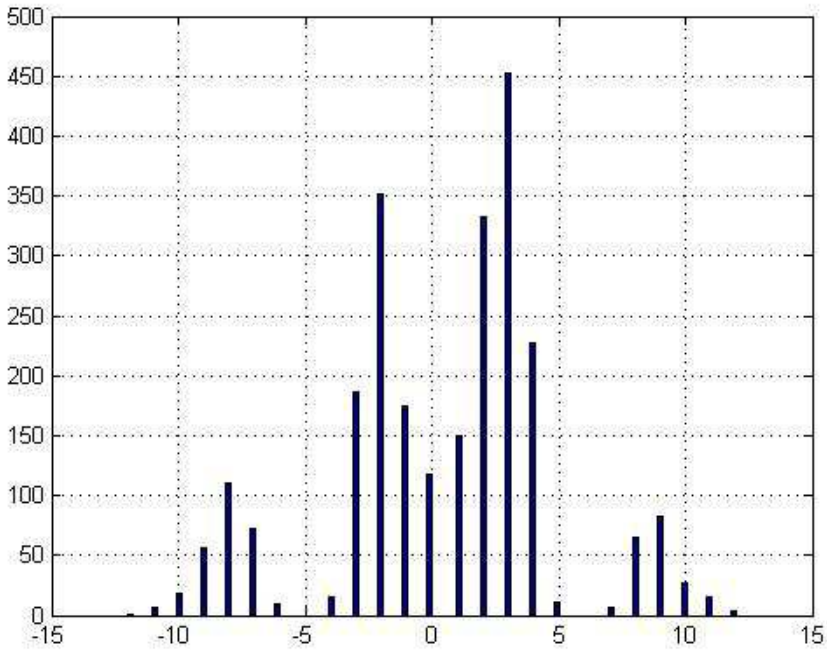


FIGURE 31. Distribution of difference in sample boundaries.

FIGURE 32 shows the spectrum of the self-interference signal at the digital baseband and the spectrum of the residual self-interference after doing frequency domain cancellation. As the cancellation is performed only for the data sub-carriers, there is higher residual at the pilot frequencies. FIGURE 33 shows the spectrum of the residual SI signal after performing the digital cancellation in time domain.

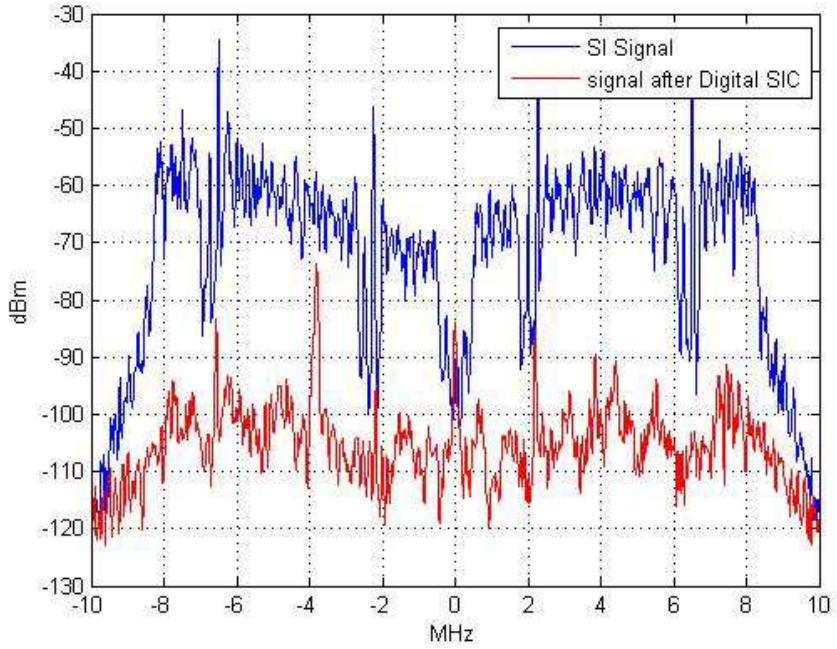


FIGURE 32. Frequency domain SIC.

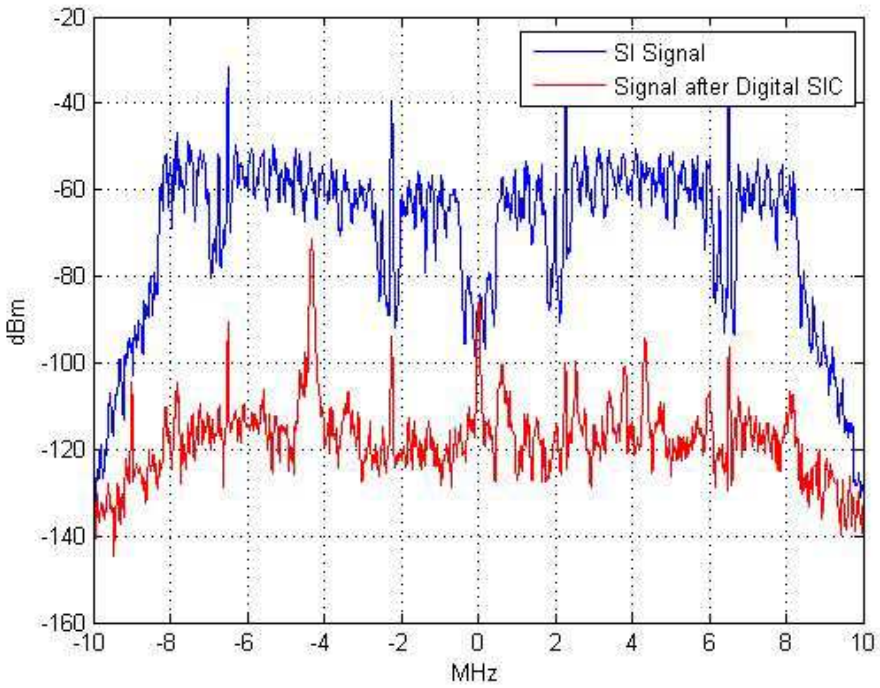


FIGURE 33. Time domain SIC.

TABLE 3 illustrates the performance of the frequency domain cancellation and time domain cancellation. The data sets used for these comparisons were provided by the dual-port antenna radio node. The data sets were from single node setup, i.e., they contain only the self-interference signal. It can be seen that for a low transmit power, both digital cancellation algorithms can cancel the self-interference up to noise floor. However, for higher transmit powers, none of the digital cancellation schemes can cancel the self-interference till the noise floor thus leaving a residual self-interference. Further details and validation numbers for time-domain and frequency domain cancellation can be found from [17].

TABLE 3. Self-interference cancellation provided by the digital block for the dual-port antenna demonstrator (BPSK modulation scheme)

Tx power	0 dBm	15 dBm
SI (SNR)	25.4 dB	43.3 dB
SIC: freq. domain	24.2 dB	26.7 dB
SIC: time domain	23.3 dB	26.1 dB

4. PERFORMANCE EVALUATION OF DUPLO DEMONSTRATOR

This section reports the results obtained from the performance evaluation of DUPLO demonstrator. In this section the validation of both full-duplex radio nodes, i.e. single-port antenna demonstrator and dual-port antenna demonstrator is described. The validation process includes the evaluation of the self-interference cancellation capabilities of the complete full-duplex transceiver as well as the demonstration and evaluation of a full-duplex wireless link. The impact of the self-interference in the received error vector magnitude (EVM), symbol error rate and constellation diagrams are analyzed for different digital modulation schemes and link distances.

The DUPLO demonstrator has been evaluated in a wireless indoor environment with people and objects moving around the full-duplex radio transceiver. By doing so, the adaptability of the analog and digital cancellation blocks to the time varying wireless channel is demonstrated. TABLE 4 depicts the main features and technical details of the scenario used for DUPLO proof-of-concept validation.

TABLE 4. Specifications for DUPLO proof-of-concept.

Feature	Specification
Scenario	Wireless point-to-point connection between two full-duplex transceivers Objects and people moving around the full-duplex radio node
Distance	Distance between nodes up to 16 meters
Carrier frequency	2.45 GHz
Signal BW	20 MHz
Transmit power	Up to 20 dBm
Type of Signal	OFDM based Waveform
Modulation Schemes	Up to 64QAM

4.1. SINGLE-PORT ANTENNA DEMONSTRATOR

The full-duplex evaluation platform builds two full-duplex radio nodes which communicate via a wireless point-to-point link. The block diagram of the evaluation platform is given in FIGURE 34. The architecture of each radio node has been described in section 2 and comprises an EBD solution presented in [2], a WiFi PIFA antenna and a WARPv3 experimentation platform. The complete system evaluation platform is controlled by a single PC. In this PC, the digital processing has been performed in MATLAB; this involves the tuning algorithm and controlling the R/C values of the balance network, calculating the SIC performance, processing of the signal frames and managing the data acquisition performed by WARPv3. In addition to that, the digital SIC is also performed in MATLAB based on the transmitted and received signal sequences. This evaluation platform enables a real full-duplex PHY link over the air.

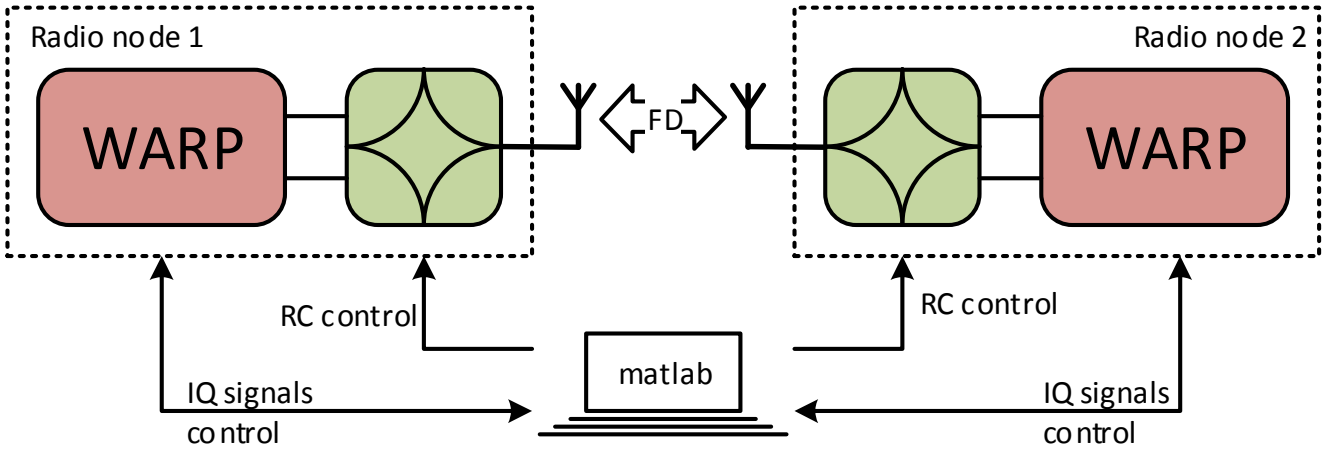


FIGURE 34. Full-duplex evaluation platform building on two full-duplex radio nodes, each comprising an electrical balance solution presented in [2].

This evaluation platform has been used over different operation conditions and environments. All measurements have been performed in an unshielded open lab environment without special precautions on the surroundings of the platform. Note that the setup has been developed for experimentation only. This means that the setup is suboptimal and is subjected performance degradation due to interconnection losses (e.g. cable, BALUN, ...), unidirectional antennas, multi-path distortion, etc.

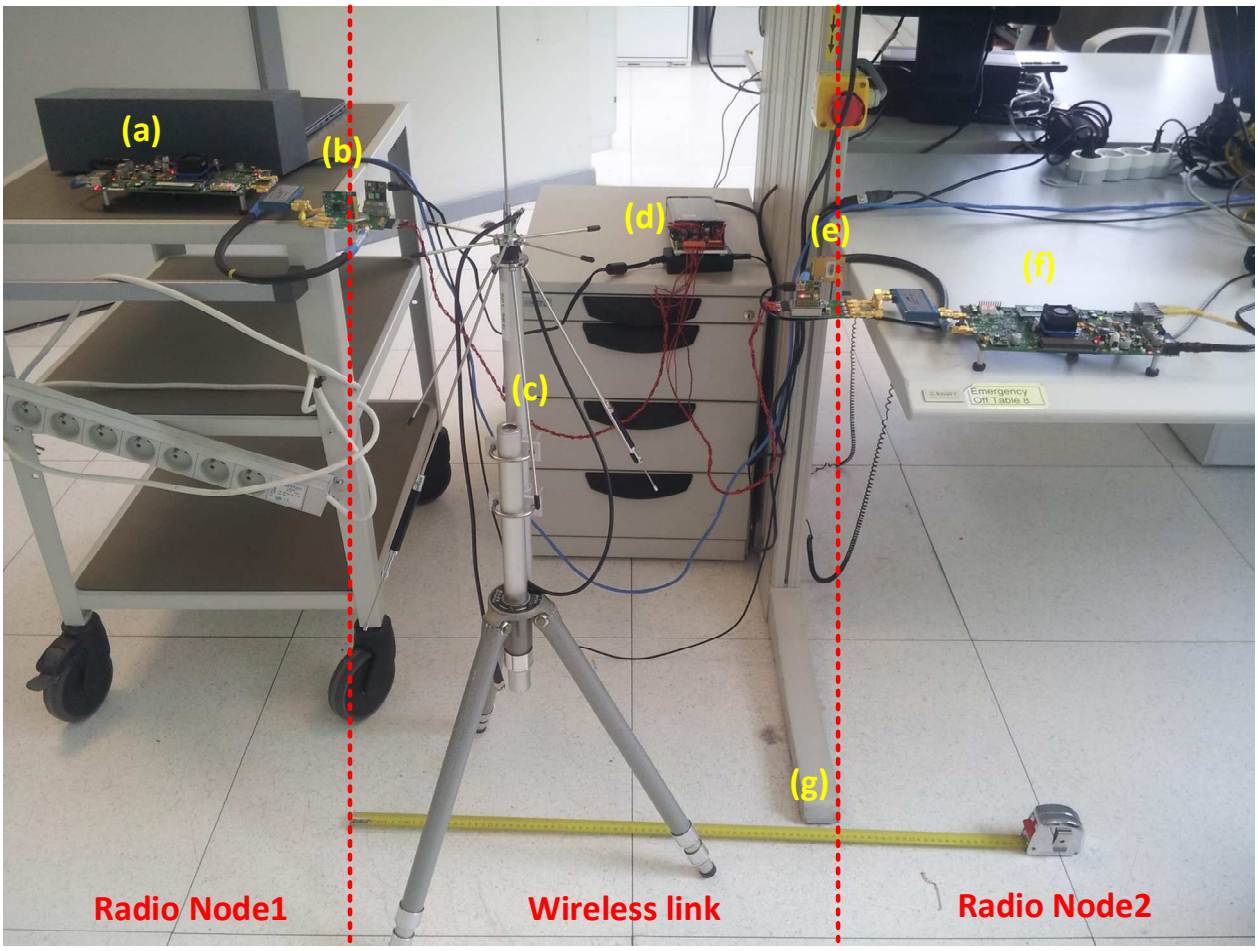


FIGURE 35. Full-duplex evaluation platform building on two full-duplex single-port antenna radio nodes.

FIGURE 35 shows a picture of the evaluation platform in operation. The Radio Node1 is located on the left and Radio Node2 is located on the right. In-between, there is a wireless point-to-point link. The system components from the evaluation platform are following:

(a) The WARPv3 platform of Radio Node1. The FPGA of the WARPv3 mainly performs data acquisition and connects to the PC via an Ethernet port. WARP is configured in FD mode, meaning that the TX and RX are simultaneously in operation on the same channel. Be aware that the TX and the RX have no common LO. This will limit the overall achievable SIC [7]. The analog TX and RX operates on the same IEEE802.11 channels in the 2.4 GHz ISM band.

(b) The EBD module, the supply module and the WiFi PIFA antenna of Radio Node1. The flexibility (including the R/C tuning of the balance network) of the EBD module is controlled via a serial protocol board which connects the module to an USB port of the PC. The differential RX output of the EBD connects to the single-ended input of WARP via a BALUN.

(c) To test the robustness of the setup and the tuning algorithm against changes in the environment, a metal object is placed at different locations close to the antennas. Given that the tuning algorithm is not implemented in the FPGA, it takes some time to execute the tuning. During this time, the environment should be static. Therefore, a tripod metal element has been used which was available in the lab. This tripod element is an unconnected antenna, but it could be any other object.

(d) The power supply module. In order to make the evaluation platform portable, a single power supply module has been used to power the complete system (except WARP). This module provides the different required supply voltages.

(e) The EBD module, the supply module and the WiFi PIFA antenna of Radio Node2.

(f) The WARPv3 platform of Radio Node2.

(g) Measures the link distance between the two radio nodes. Different distances have been measured as illustrated later.

To enable a clear interface for the user to control the evaluation platform and to observe the main performance results, a GUI has been developed as illustrated in FIGURE 36. The plots in this figure are continuously updated based on effective measurements, and any change of parameter by the user will be taken into account. Given that the signal processing is performed in MATLAB (and not in the FPGA), one should expect a certain processing time.

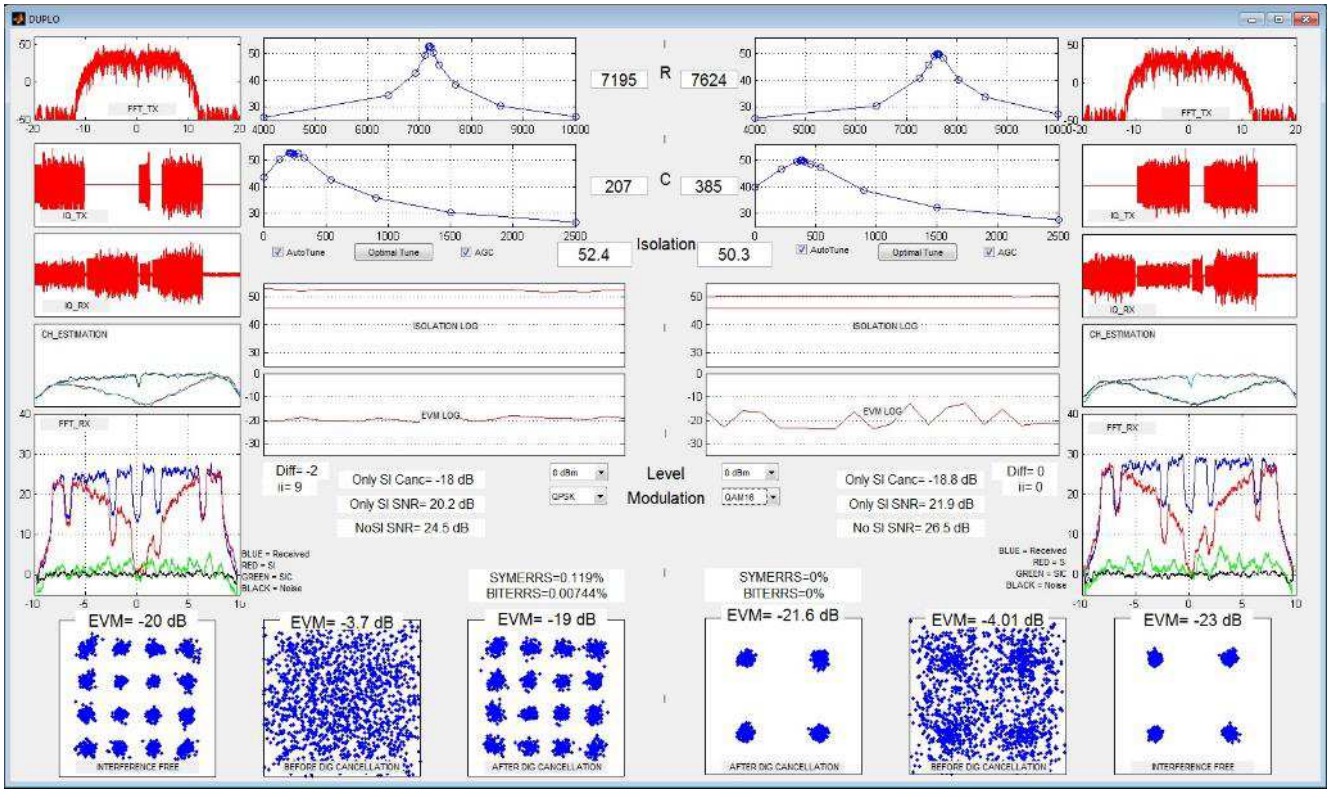


FIGURE 36. Graphical User Interface (GUI) of the full-duplex evaluation platform with two full-duplex single-port antenna radio nodes (comprising EBD solutions).

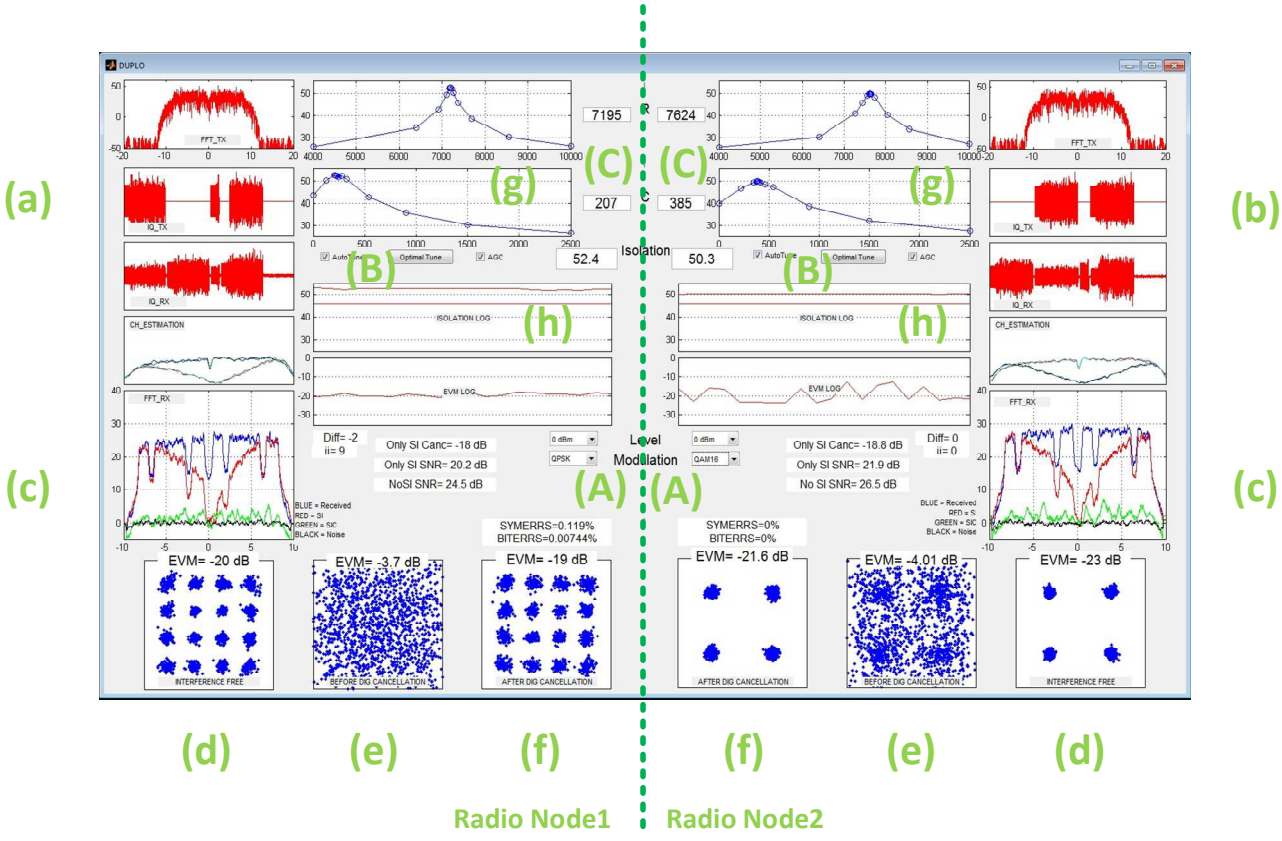


FIGURE 37. GUI of the full-duplex evaluation platform, including indications for a more detailed explanation

FIGURE 37 is the same as FIGURE 36, but indications are added for further explanation.

The GUI offers the user to control and modify the operation of the experimentation platform:

(A) Selection of the modulation scheme (BPRK, QPSK, QAM16, QAM64) and the transmit power. This power corresponds to the WARP setting and not to the effective power at the antenna. This power selection also offers to deactivate the radio node. In this way, single node measurements can be performed.

(B) Activation/deactivation of the self (or automatic) tuning of the balance network in case the antenna impedance causes the RF SIC to be lower than the threshold. The knob 'Optimal Tune' tunes the balance network for best balance condition. This tuning results in a better RF SIC which stops retuning when the SIC threshold is reached, but requires more tuning steps. Also, the AGC of the receiver can be activated/deactivated. Note that the gain is determined per burst, thus covering both the FD and HD operation.

(C) The R/C values (digital code) can be filled in manually.

The GUI provides a lot of measurement results and information on the experimentation platform settings to enable in-depth analysis. There are several similarities with the GUI of the dual-port antenna demonstrator to enable easy comparison. The GUI provides the following outputs:

(a) Raw signal plots, covering the transmitted signal (both in time and in frequency), the time domain received signal. These time domain plots clearly illustrate the signal structure of HD and FD operation, and it shows the signal strengths of the received and the SI signal.

(b) Similar signal representation, but of the other radio node. Note the difference in transmitted signals to obtain HD operation for calculation of the digital cancellation SIC etc.

(c) The spectral representation of the received signals after the FFT of the receiver. The blue curve shows the received signal when operating in HD, the red curve shows the received signal when operating in FD (without digital cancellation), the black curve shows the measured spectrum of the noise (measured on the signal burst when no signal is transmitted by either node) and the green curve shows received signal in FD operation after digital cancellation. These spectral curves give a good indication of the SIC performances and the SNR's.

(d) The constellation diagram and EVM performance of the HD part of the received signal burst. This EVM is a benchmark to value to FD EVM performance, but the FD EVM cannot exceed the HD EVM.

(e) The constellation diagram and EVM performance of the FD part of the received signal burst without digital cancellation. Note that this EVM can be large in case the RF SIC is not sufficient. In case the EVM exceeds about 5 to 7 dB, the EVM values are no longer accurately relevant.

(f) The constellation diagram and EVM performance of the FD part of the received signal burst with digital cancellation. This represents the performance of the FD radio node.

(g) These graphs (upper and lower) show the measured SIC values over the measured R/C code combinations. These graphs illustrate the measurement points of the tuning algorithm. These curves are dynamic when the tuning is active. The R/C values (codes) used at each time instance are given in the (editable) fields (C).

(h) The upper and lower curves give the log of the SIC and the EVM over time. The straight line in the upper curve (SIC) is the SIC threshold. If the SIC value becomes lower that this threshold and if the "Auto tune" is activated, the tuning algorithm will be activated, and the measurement points of the algorithm (over the R/C codes) will be illustrated in (g).

Also other results are illustrated, but they are less relevant for this document.

4.1.1. RF self-interference

The RF SIC is obtained by having a balanced condition between the antenna impedance and the balance network. The SIC value is checked during each communication burst according to a threshold, which is set to 48 dB in current experiments. If this value is not reached, the tuning algorithm is activated and the R/C values are tuned. The tuning capabilities and the obtained RF SIC have been tested over different environmental conditions, i.e. by placing objects in the far and near surroundings of the antennas. It has been observed that, as long as the antenna impedance is within the coverable range of the balance network, the threshold of 48 dB is reached. The GUI displays the log of the SIC over time in FIGURE 37 (h).

4.1.2. Link distance

The system performance has been measured over different link distances. In all measurements, it is observed that the EVM performance of Node1 is worse than of Node2. Different experiments have been performed (including swapping the radio hardware) to tackle this issue. This issue was however not resolved, and it seemed not to be related to the hardware. Given the difference was relatively small, this issue was tolerated.

FIGURE 38 illustrates the EVM performance versus the link distance. The series EVMNode1/2 illustrates the EVM performance during full-duplex operation measured at the corresponding radio node. The series EVMnoSI illustrate the EVM in half duplex operation, meaning that the radio node receives signals from the other node, while not transmitting any data simultaneously. It is observed that there is a minor almost constant difference in EVM between the FD and HD operation. At distances shorter than 40 cm, the EVM performance is best, while between 40 cm and 80 cm, the EVM stagnates around -15 and -17 dB for the corresponding radio nodes. Beyond 100 cm, both the HD and FD EVM are flooring at -7 and -6 dB. This flooring is caused by the limited transmit power to cover the distance. To overcome this issue, the transmit power has been increased from 0 dBm to 6 dBm in FIGURE 39. It can be observed that due to this increase, the EVM performance of the HD operation is improved with about 5 dB. Unfortunately, this improvement is not obtained in FD operation. On the contrary, the EVM performance degrades with about 5dB. This indicates a linearity issue when operating in FD. This will be further analysed further in this document.

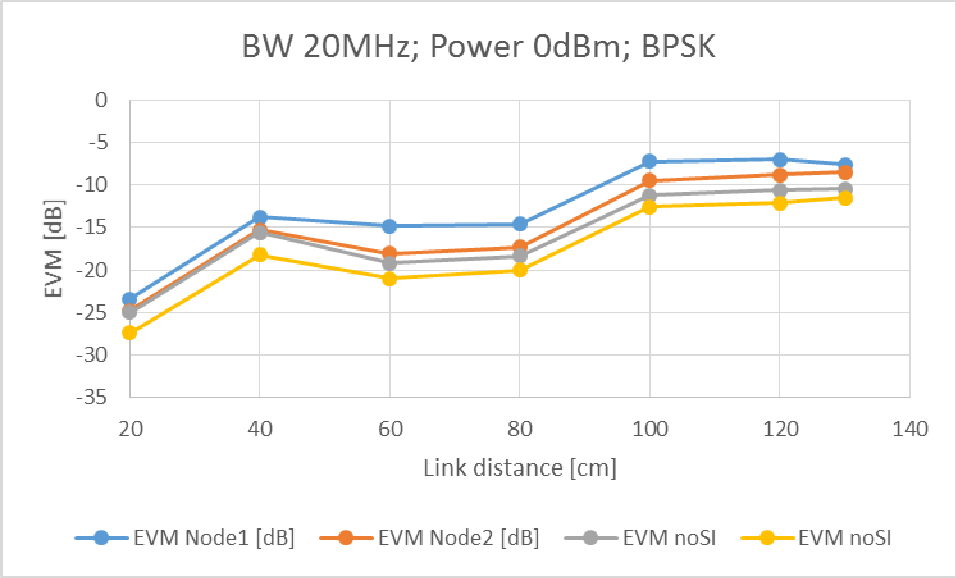


FIGURE 38. EVM versus the link distances.

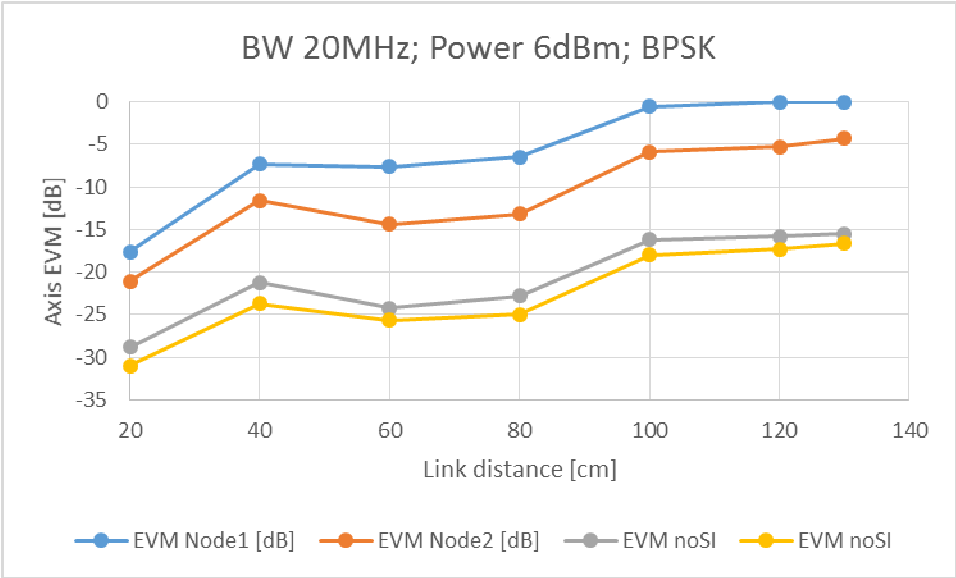


FIGURE 39. EVM versus the link distances with an increased transmit power.

4.1.3. Bandwidth

Based on [2], it was discussed that the average SIC performance degrades with increased bandwidth. In order to explore if the SIC improves when decreasing the bandwidth, an alternative signal with a reduced bandwidth has been implemented. To maintain all signal characteristics at a lower bandwidth, and given that WARP does not allow internal resampling, the length of the alternative signal increases. Due to this increased length, the bandwidth could only be halved in order not to exceed the buffer length implemented in WARPLab 7.4. When comparing FIGURE 40 with FIGURE 38, almost no differences can be observed both in FD and HD mode. When comparing FIGURE 41 and FIGURE 39 however, an improvement of about 5 dB is observed in FD operation, while there is no real improvement in HD operation. This similarities and differences are explained by the fact that the bandwidth impacts the SIC, and that the EVM is not always determined by the SIC (only). As there is no SI in HD, it is not expected that the EVM improves with improved SIC. In FD, the SIC will have an impact on the EVM in case the SI contributes to the EVM degradation. In our example, the SI (after cancellation) is large enough to degrade the EVM. Therefore, the EVM improves when the SIC improves (due to a reduced bandwidth).

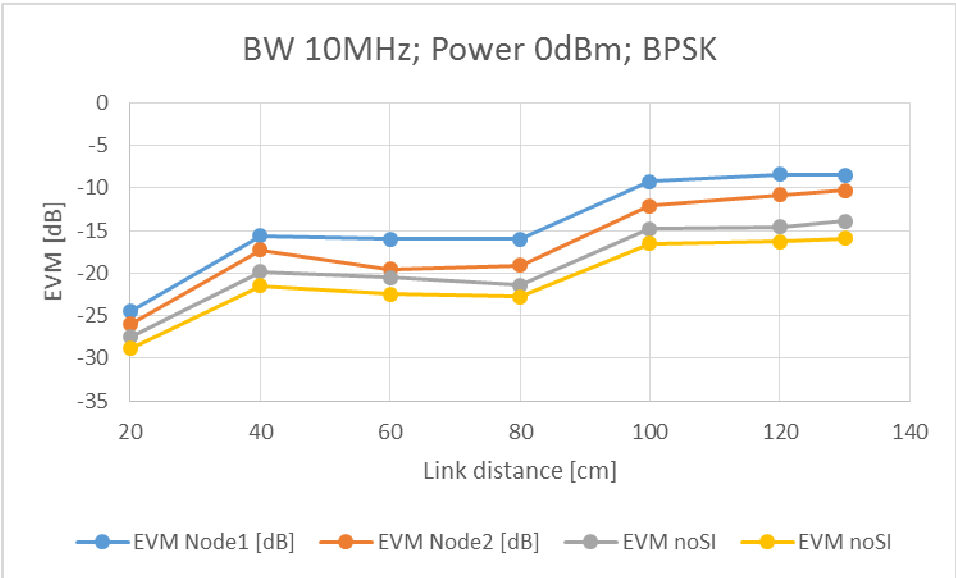


FIGURE 40. EVM versus the link distances with a bandwidth of 10 MHz (instead of 20MHz).

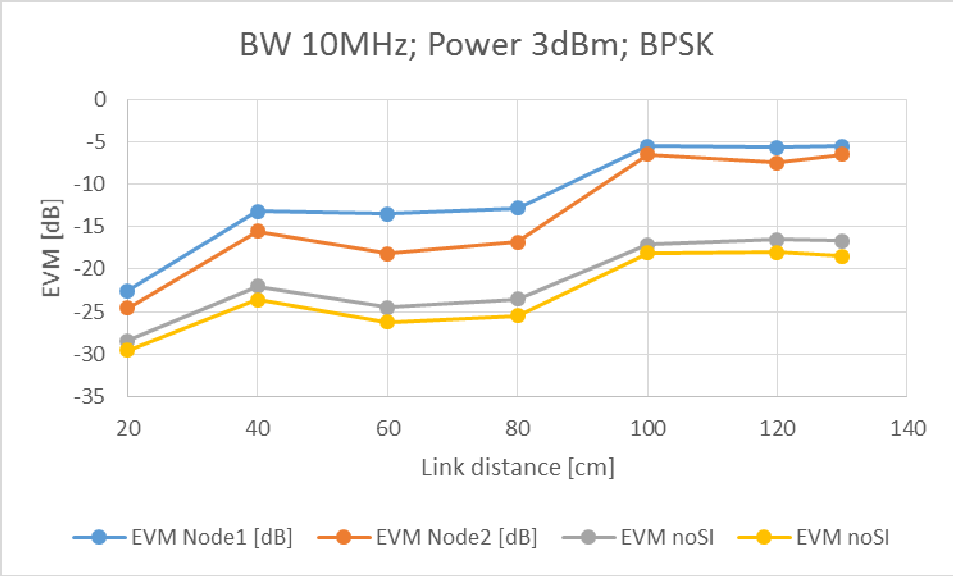


FIGURE 41. EVM versus the link distances with a bandwidth of 10 MHz (instead of 20MHz) and an increased transmit power.

4.1.4. Transmit power

In section 4.1.2, it has been noticed that the transmit power can improve the EVM performance and eventually increase the link distance. The measurements in section 4.1.2 however indicate that this is only the case in HD operation in case the transmit power increases from 0 dBm to 6 dBm. In this section, the effect of the transmit power on the EVM performance is elaborated. FIGURE 42 illustrates the relation between the EVM performance and the transmit power. In HD operation, the EVM scales linearly with the transmit power. This is expected as an increased transmit power will result in a better SNR at the RX of the other radio node. In case the transmit power is lower than 0 dBm, this trend is also represented in FD operation. At higher power, however, the FD EVM performance degrades due to SI. As the FD EVM continues to degrade with increased power, the receiver seems not yet completely clipped.

FIGURE 43 indicates the impact of the link distance. As expected, with a shorter link distance, the remote node will degrade the EVM performance of the local node in HD operation due to saturation. This performance degradation is visible with transmit powers higher than 5 dBm with a link distance of 20 cm.

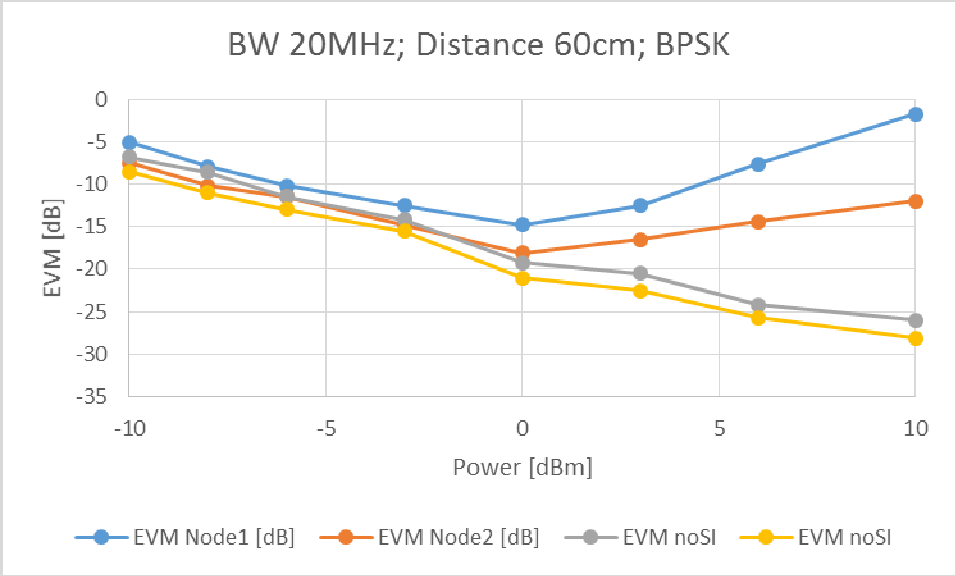


FIGURE 42. EVM versus the transmit power.

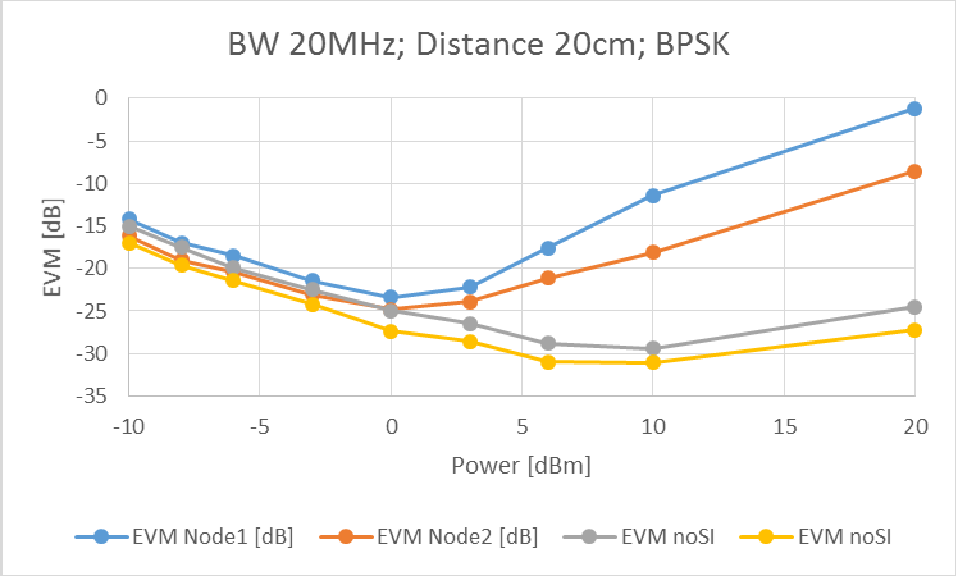


FIGURE 43. EVM versus the transmit power with a shorter link distance (20 cm instead of 60cm).

4.1.5. Unequal transmit power

In order to differentiate the distortion between the two radio nodes, a similar experiment as in section 4.1.4 has been performed, but now with an unequal transmit power. FIGURE 44 and FIGURE 45 illustrate the EVM performance in function of a transmit power sweep of one radio node, while the other node keeps a constant power of 0 dBm. As expected, both figures show a very similar behaviour. In FIGURE 44, the transmit power of radio node 1 sweeps, while the power of node 2 is fixed to 0 dBm. The power sweep of node 1 is clearly visible in the received EVM of node 2 (EVM Node2). As this relation is linear, this EVM is not hampered by the SI in node 2, although node 2 is operating in FD (with a fixed power). This also indicates that the transmitter linearity of node 1 is maintained over the complete power range. When observing the EVM performance of the node 1 receiver, it is observed that in HD operation, the EVM is almost constant. This is to be expected as the transmit power of remote source (node 2) is constant. In FD operation, however, the EVM performance degrades when its own transmit power equals 0 dBm and more. This clearly indicates that the receiver of node 1 is subjected to SI signals caused by its own transmitter. Most probably, these SI is caused by limited linearity

in the balance network as described in [2]. Similar behaviour is observed in FIGURE 45, but with the opposite nodes.

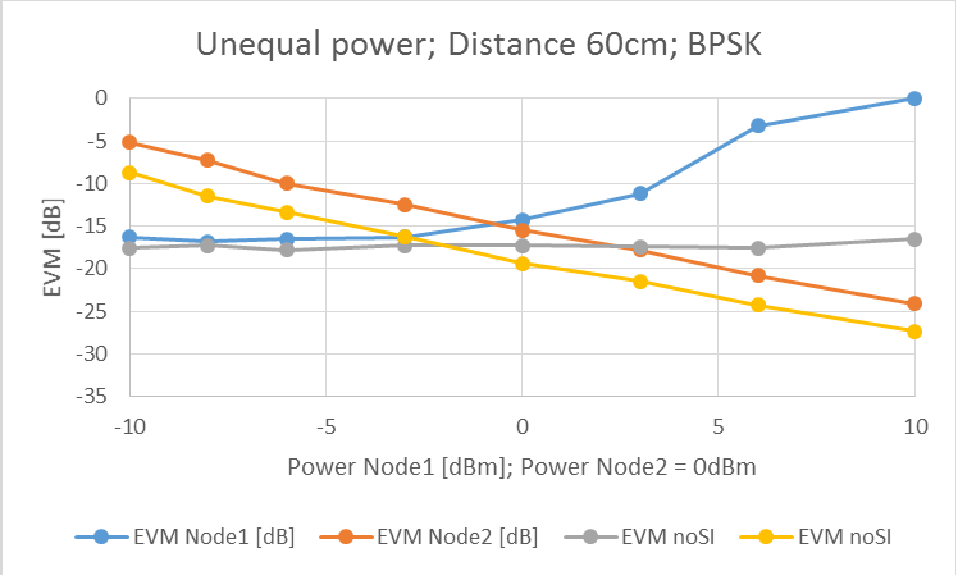


FIGURE 44. EVM versus the transmit power of Node1, while keeping the power of Node2 constant.

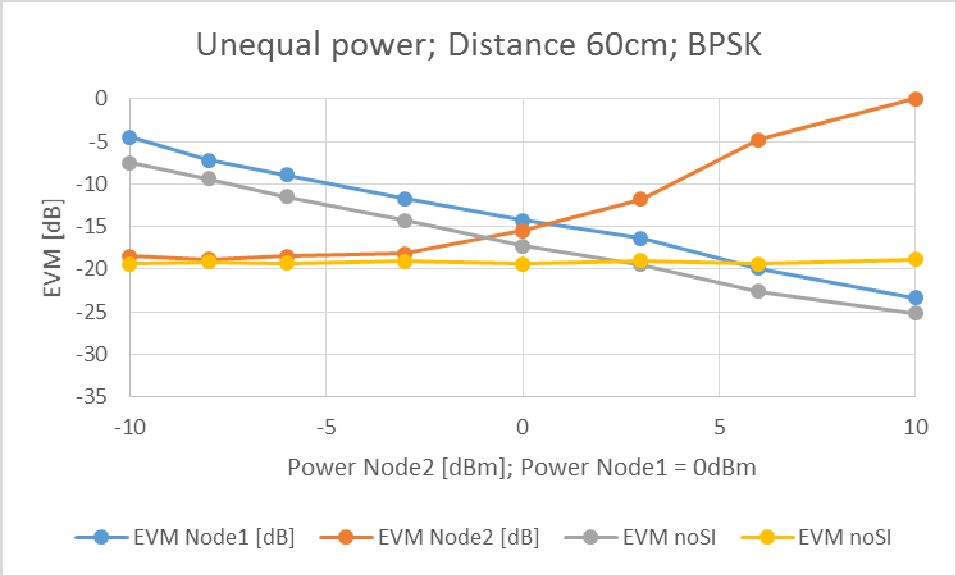


FIGURE 45. EVM versus the transmit power of Node2, while keeping the power of Node1 constant.

4.1.6. Modulation scheme

All previous measurements have been performed with BPSK modulation as the modulation scheme has a limited impact on the EVM. Higher modulation schemes result in a minor increase in the peak-to-average power ratio, but it is not expected that this will be visible in the EVM measurements obtained with the considered experimentation platform. The modulation scheme will, however, have an impact on the digital error rates such as the bit error rate and the symbol error rate. FIGURE 46, FIGURE 47 and FIGURE 48 illustrate the measured bit and symbol error rate in both FD radio nodes for IEEE802.11 signals with a bandwidth of 20MHz. Note that the error values are quantified based on the limited amount of symbols and bits in a single data burst. This is in conflict with the statistical requirement to average over a large amount of

samples/symbols/bits, especially with a small amount of errors. Therefore, the results in FIGURE 46, FIGURE 47 and FIGURE 48 are only indicative.

FIGURE 46 indicates a slight increase of the errors with a low transmit power (below -6 dBm). That is because the transmit power is too low to cover the link distance. In the range between -5 and 5 dBm, no errors are observed. At higher powers, the errors increase due to SI. Note however that overall the amount of errors are limited (smaller than 12 %). FIGURE 47 and FIGURE 48 show a similar behaviour but with an increased error rate. It is remarkable that the symbol error rate for node 1 is substantially higher compared to node 2. This requires further investigation in the future.

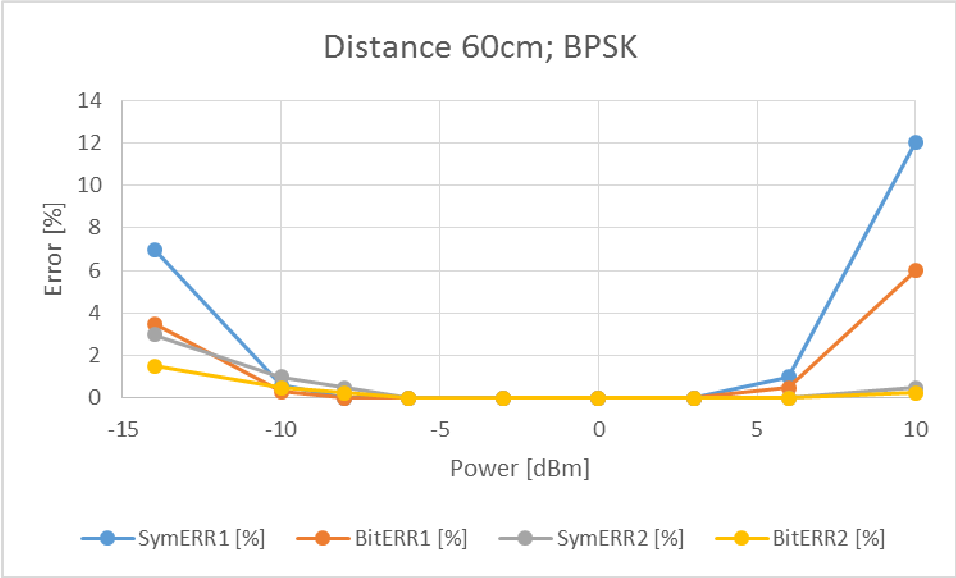


FIGURE 46. The symbol and bit error in function of the transmit power with BPSK modulation.

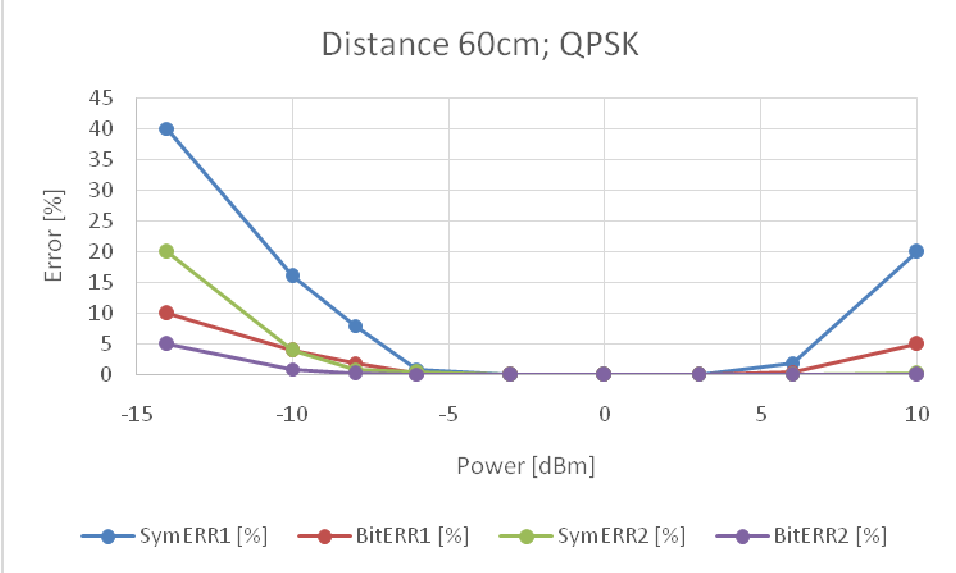


FIGURE 47. The symbol and bit error in function of the transmit power with QPSK modulation.

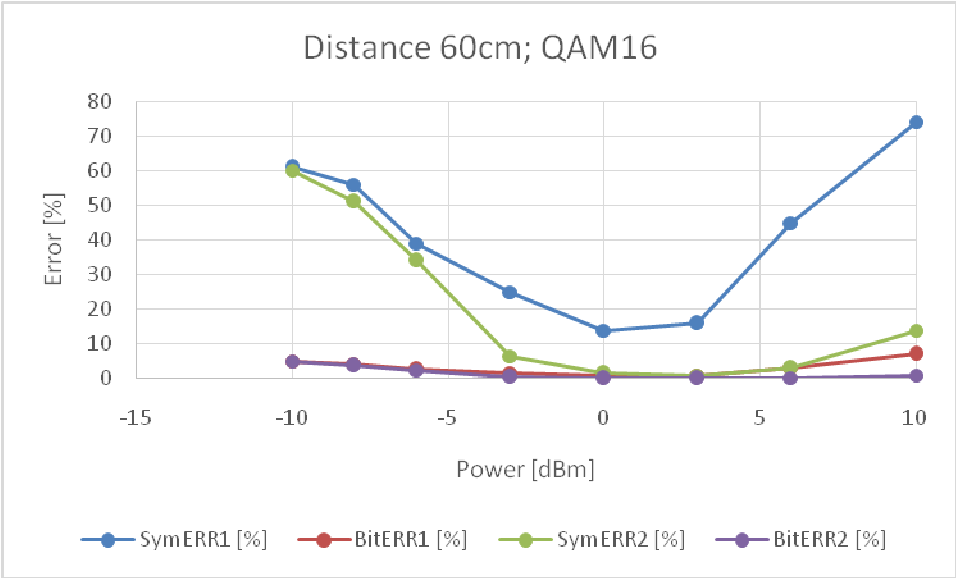


FIGURE 48. The symbol and bit error in function of the transmit power with QAM16 modulation.

4.1.7. Reduced RF self-interference cancellation

As described in section 4.1.1, the RF SIC is maintained by tuning the balance network depending on the SIC threshold. The GUI also allows to switch-off the self-tuning mechanism and to maintain the R/C values even when the antenna impedance changes. In this way, the RF-SIC is deliberately reduced.

FIGURE 49 illustrates the reference scenario with auto tuning activated. In radio node 1, a SIC of 50.2 dB is obtained. The spectral plot illustrates the desired signal in the node 1 receiver. This signal has been transmitted by the radio node 2 and propagated through the wireless channel. The desired signal has an EVM of -15.3 dB when node 1 is not transmitting anything (HD operation). This performance is indicated in the first constellation diagram. This EVM value corresponds with the average power ratio between the desired signal (blue spectrum) and the receiver noise (black spectrum). When operating in FD, the RF self-interference (red spectrum) is added to the desired signal (blue spectrum), degrading the EVM to 4.5 dB (second constellation diagram). This size and shape of the SI is determined by the SIC offered by the RF-IC. Then, the digital cancellation will further suppress the SI signal to the green spectrum, resulting to a final EVM of -12.1 dB, as illustrated in the third constellation diagram. This EVM value is relatively close to the HD performance, and the average power of the green spectrum is approaching the average power of the black spectrum. Based on these results, the following SIC values are obtained:

- RF SIC = 50.2 dB
- digital SIC = 4.5 + 12.1 = 16.6 dB

⇨ Total SIC = 66.8 dB

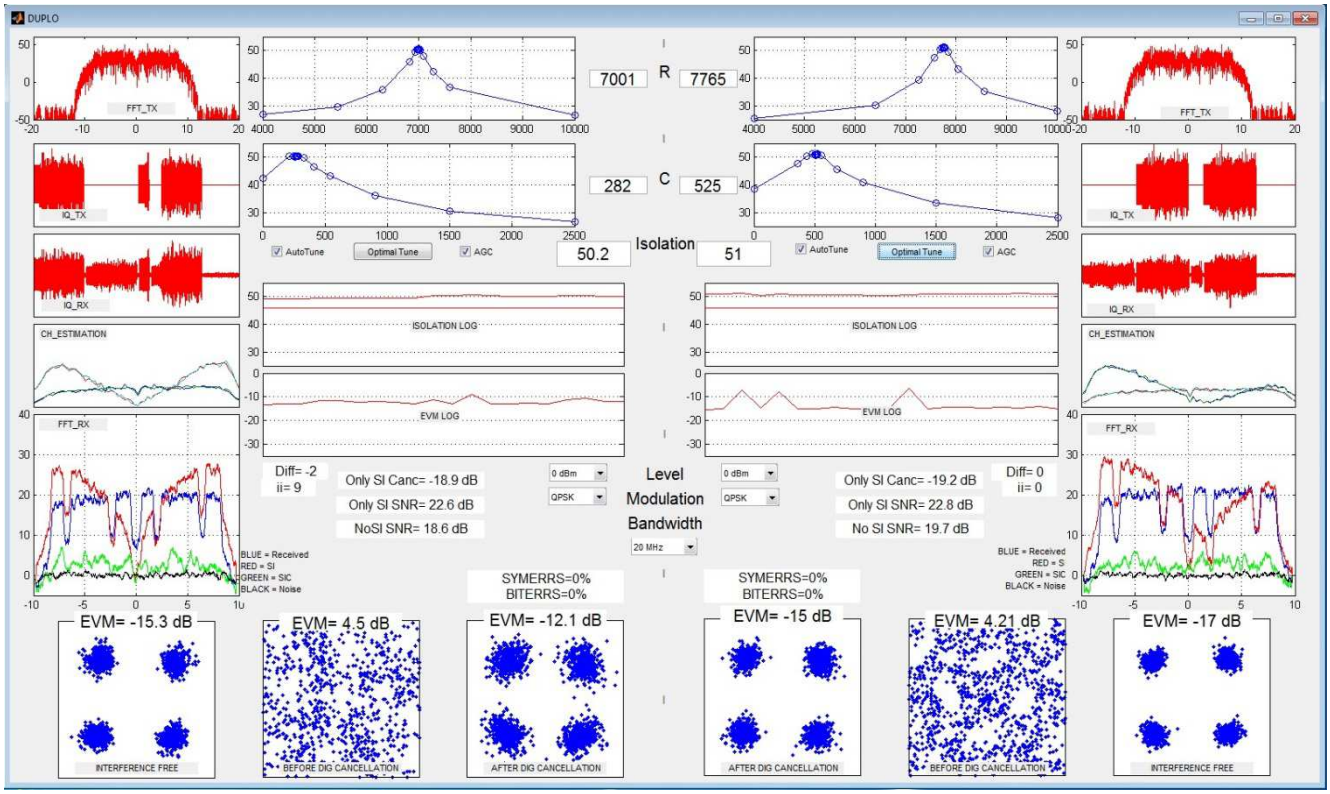


FIGURE 49. Reference scenario for illustrating the digital cancellation performance.

Now, the impact of a reduced RF-SIC is investigated by switch-off the self-tuning of the RF-IC in radio node 1 and by changing the surroundings of the antenna (thus changing the antenna impedance). To prevent clipping in the receiver path due to an increased SI, the ACG will change the gain settings in the receiver. Two scenarios are considered as illustrated in FIGURE 50 and FIGURE 51. In the first scenario, a moderate SIC reduction is applied, resulting in a RF SIC of 40.8 dB. Therefore, as illustrated in the spectral graph, the SI after the RF SIC is increased compared to the desired signal measured in HD. This increased SI activates the AGC and modifies the receiver gain settings both in HD and FD mode. Therefore, the SNR of the HD desired signal with respect to the receiver noise decreases. Although the EVM after RF SIC is very bad (i.e. 18.7 dB is indicated, but this value is not really relevant as the EVM calculation is not accurate above ~7 dB), the digital cancellation succeeds to suppress the SI signal, resulting in an EVM of -6.75dB. In the second scenario, the RF SIC is further degraded to 34.9dB, resulting in an increased difference between the SI power after RF SIC compared to the HD desired signal. Again, in order to avoid saturation in the receiver, the receiver gain is changed, resulting in a HD EVM of -6.19 dB. Although the digital cancellation further reduced the SI with about 17 dB, the resulting EVM is 0.375 dB only. This poor EVM performance is also visible in the spectral plot: the remaining SI power is similar to the desired signal power.

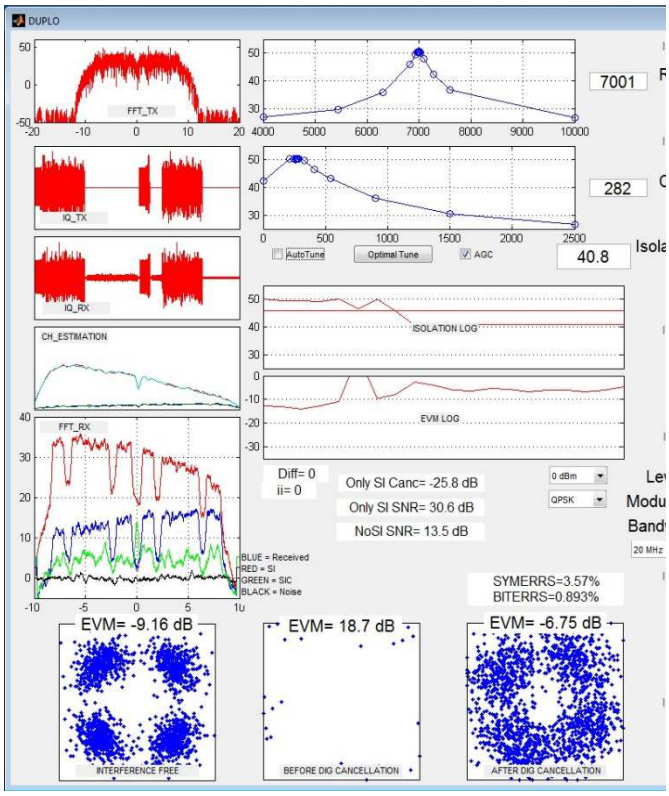


FIGURE 50. Scenario 1 - with reduced RF SIC.

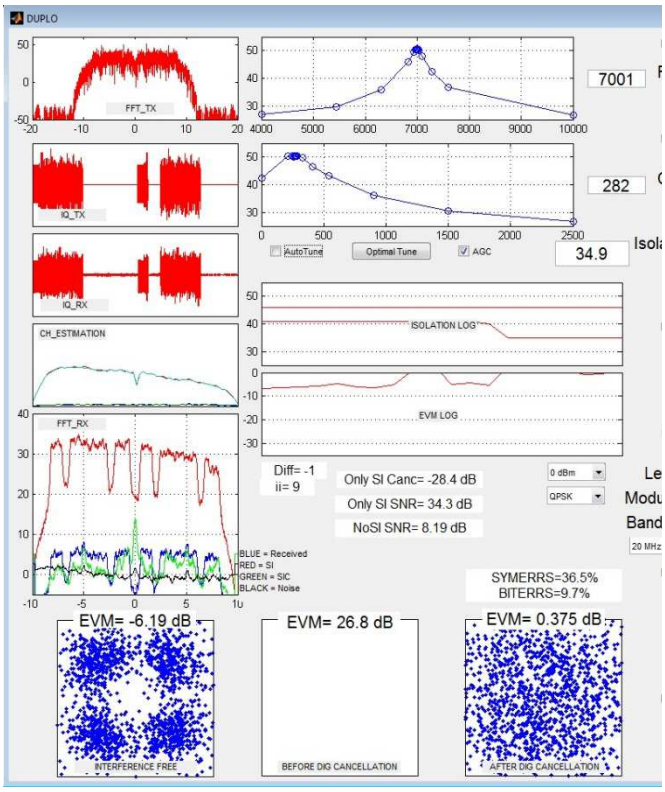


FIGURE 51. Scenario 2 - with strongly reduced RF SIC.

4.2. DUAL-PORT ANTENNA DEMONSTRATOR

This section reports the performance evaluation of the dual-port antenna demonstrator. Two full-duplex radio nodes were separated different distances, while both transceivers were connected to a control PC as FIGURE 52 illustrates. The full-duplex baseband and digital cancellation block runs on the control PC, while it also sends the activation command to the microcontroller when it is necessary to tune the active cancellation network. This measurement setup has been used to evaluate the performance of the full-duplex wireless link. Moreover, this setup has been also used to quantify the cancellation capabilities of the transceiver. This corresponds to the single-node setup described in section 2.3 where only one of the radio nodes is operating in full-duplex (only the self-interference signal is in the receiver). FIGURE 53 shows a picture of the evaluation platform build on two dual-port antenna radio nodes when the distance between nodes is 1 meter approximately.

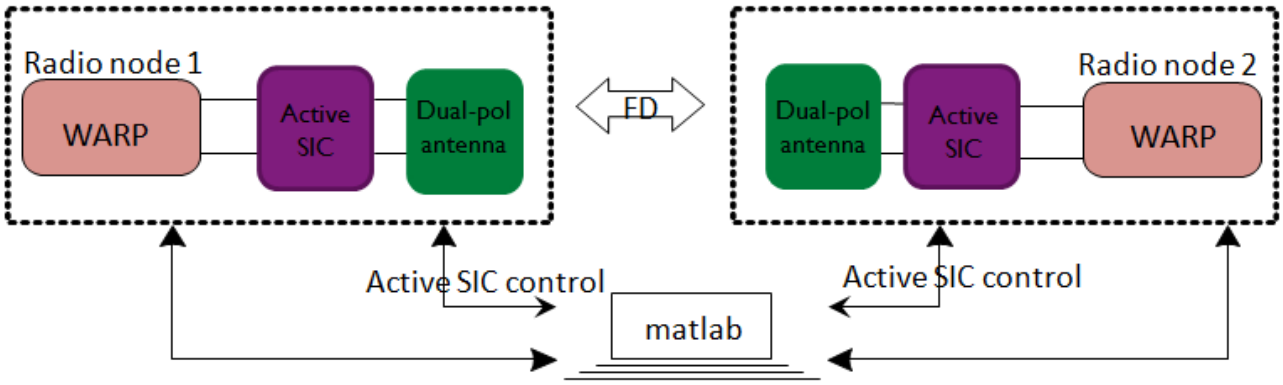


FIGURE 52. Measurement setup for the evaluation of the full-duplex wireless link.

FIGURE 53. Picture of the evaluation setup with the dual-port antenna radio node.

4.2.1. Cancellation capabilities of the full-duplex transceiver

The total self-interference cancellation provided by the dual-port antenna radio node has been evaluated using the single-node setup described in section 2.3. FIGURE 54 illustrates the self-interference cancellation for different transmit powers when the dual-port antenna demonstrator is in the moderate multipath scenario. As in the experiments reported in section 3.2.4, we conduct 30 runs for each PTX and we calculated the mean SIC over the signal bandwidth, i.e. 20 MHz. As can be seen from the obtained results, the digital cancellation improves in 30 dB the cancellation at analog level, increasing up to 85-90 dB the total amount of SIC provided by the overall radio transceiver (this performance in terms of cancellation has also been verified with the dual-node setup described in section 2.3).

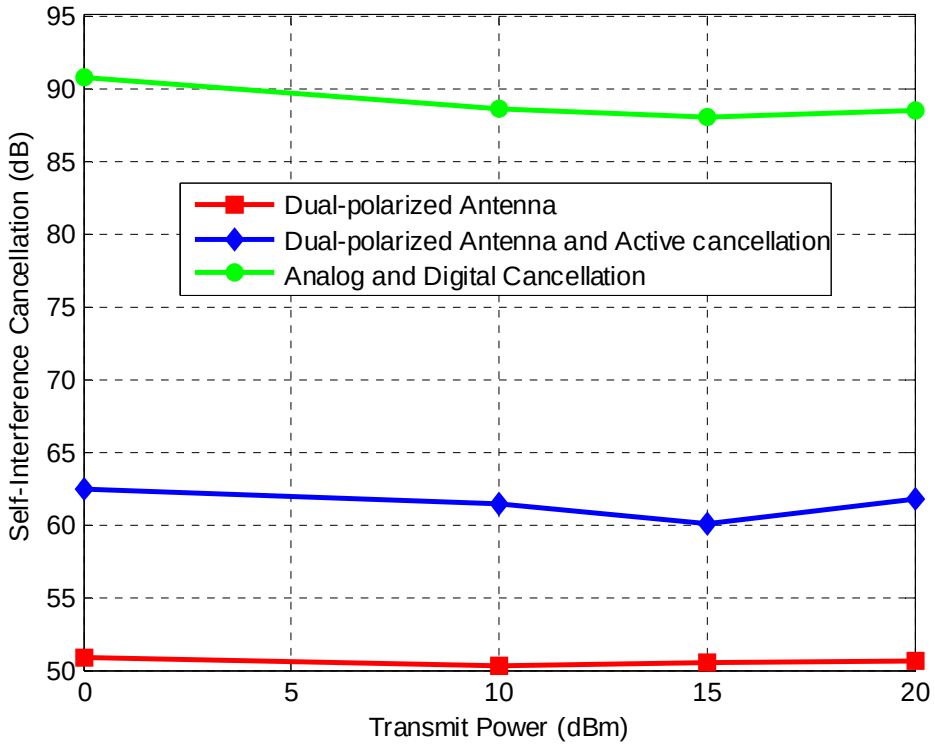


FIGURE 54. Self-interference cancellation provided by the dual-port antenna radio node (moderate multipath scenario).

FIGURE 55 shows the spectrum of the self-interference signal after analog (ASIC) and after digital (ADSIC) cancellation blocks when a BPSK modulated signal is transmitted and the PTX is 0 dBm. As can be seen, digital cancellation achieves to cancel the remaining self-interference signal till the receiver noise floor which is around -85 dBm.

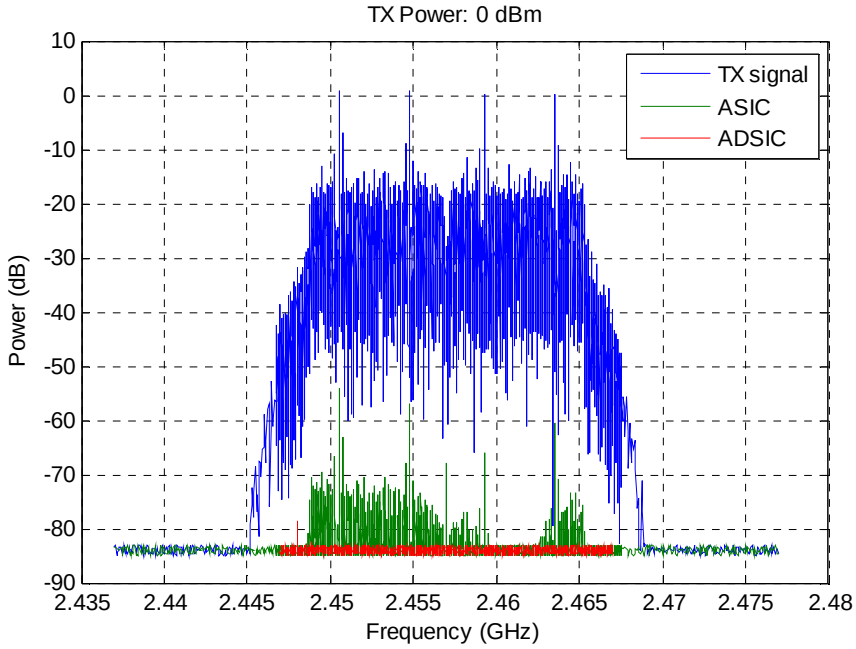


FIGURE 55. Spectrum of the residual self-interference signal after analog and digital cancellation stages.

In addition, the dual-port antenna radio node performance in terms of self-interference cancellation has been also evaluated under the different scenarios described in section 3.2.4. The cancellation provided by the complete transceiver is practically the same in all the scenarios, and only a minor degradation less than 5 dB is observed when the worst case scenario is considered, i.e. when metallic objects are placed close to the dual-polarized microstrip antenna, as FIGURE 56 illustrates.

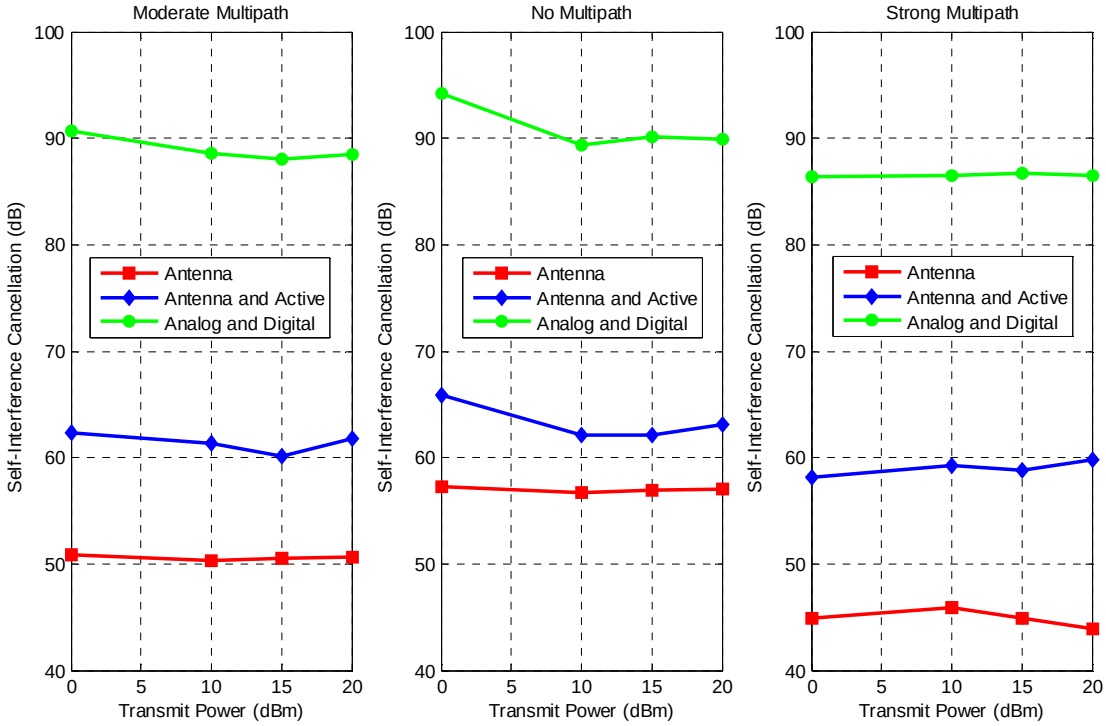


FIGURE 56. Self-interference cancellation provided by the dual-port antenna demonstrator in different scenarios.

Finally, the adaptability of the analog cancellation solution to the changes in the environment close to the full-duplex transceiver has been also evaluated. FIGURE 57 shows the evolution of the self-interference in time (a time slot of 30 seconds is shown) when different objects (metallic objects, hand-effect) are placed close to the antenna. The active cancellation network is re-tuned (and new attenuation and phase coefficients are calculated) when the analog SIC drops below 50 dB, when objects are placed close to the full-duplex radio node at the instants of time 10 and 18. As can be seen from FIGURE 57, the analog SIC is above the predefined threshold of 50 dB after re-tuning.

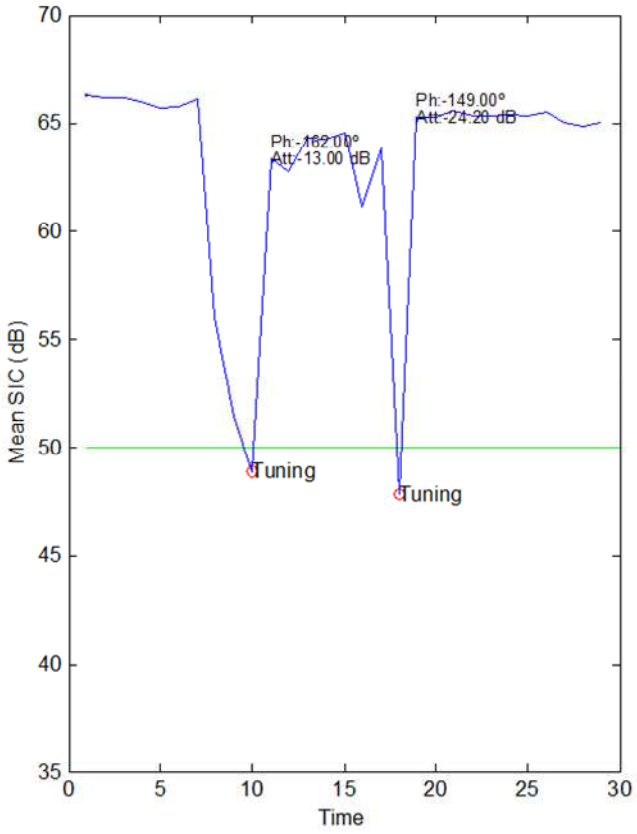


FIGURE 57. Analog self-interference cancellation in time.

4.2.2. Full-duplex wireless link demonstration

This section reports the performance of the full-duplex wireless link between two dual-port antenna radio nodes separated different distances. FIGURE 58 shows the graphical user interface developed for the evaluation of the full-duplex wireless link with two dual-port antenna radio nodes. The information presented in this GUI is similar to the information shown in the single-port antenna demonstrator and described in section 4.1. The left side of the GUI contains the information related to node1 while the right side contains the information related to node 2. The data results represented in the GUI is the same for both nodes and it consists of:

1) Channel estimations for self-interference channel and desired signal channel.

2) Self-interference cancellation at analog level in time

3) Self-interference signal spectrum after analog cancellation (ASIC), after analog and digital cancellation (ADSIC) and the spectrum of the received signal in half-duplex mode (HD).

4) Transmitted signals in time domain. Moreover, this picture also includes the self-interference cancellation provided by digital algorithms (SIC in red), the self-interference signal-to-noise ratio (SI(SNR) in red), the measured symbol error rate (SER in green) and the signal-to-noise ratio of the desired signal (Des(SNR) in green).

5) Received constellation diagrams. The red points represent the received constellation when only analog cancellation is applied, the green points represent the received constellation when both analog and digital cancellation are applied and blue points represent the received constellation when nodes operate in half-duplex mode. For each constellation diagram, the value of the EVM is also represented in this figure.

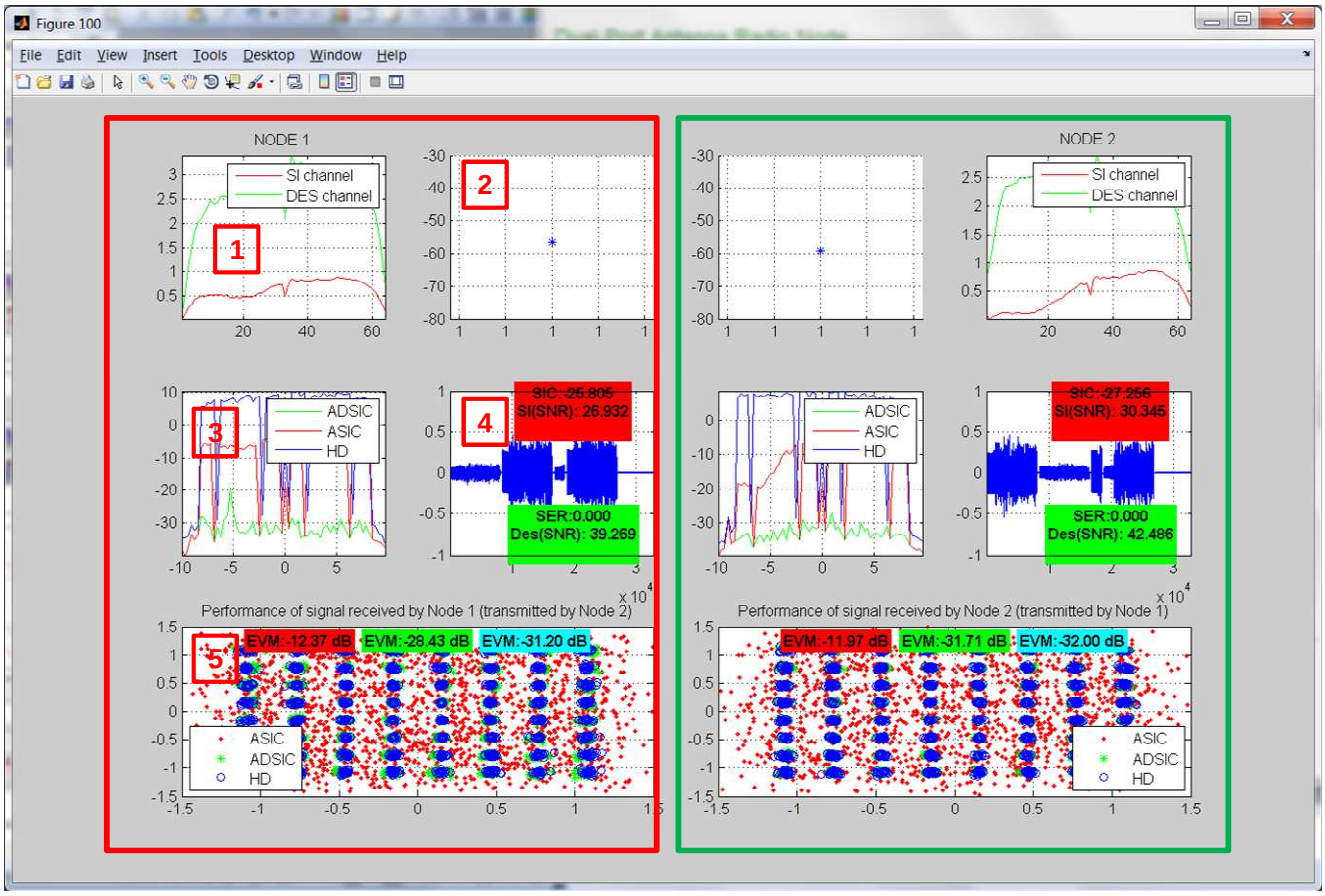


FIGURE 58. Graphical User Interface for the evaluation of the full-duplex wireless link.

As in the single-port antenna demonstrator, the signal processing is performed in MATLAB (and not in the FPGA), therefore one should expect a certain processing time when visualizing the results in this GUI.

4.2.2.1. *Impact of analog SIC on the FD link performance.*

Firstly, the impact of the self-interference on the link performance is evaluated. For that purpose, the two FD radio nodes were separated 1 meter of distance while one of the nodes was configured to provide different levels of analog SIC (the settings of the analog controlled attenuator and phase shifter were modified in order that active cancellation network provides different self-interference cancellation levels). Afterwards, the link performance in terms of EVM (when only analog cancellation is applied) was measured for a QPSK modulated signal, as FIGURE 59 illustrates. The transmit power is 0 dBm at both radio nodes.

The self-interference increases the receiver noise floor and the reception performance degrades, as can be seen in the constellation diagrams shown in FIGURE 60(A) (in red - EVM when only analog cancellation is applied). Contrarily, the tuning of the analog cancellation solutions improves the reception performance of the wireless link towards an error vector magnitude of -15 dB, as FIGURE 60(B) depicts (in red).

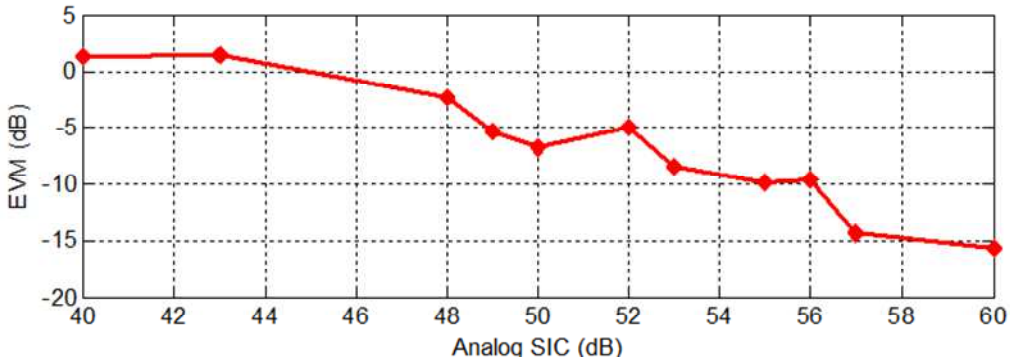
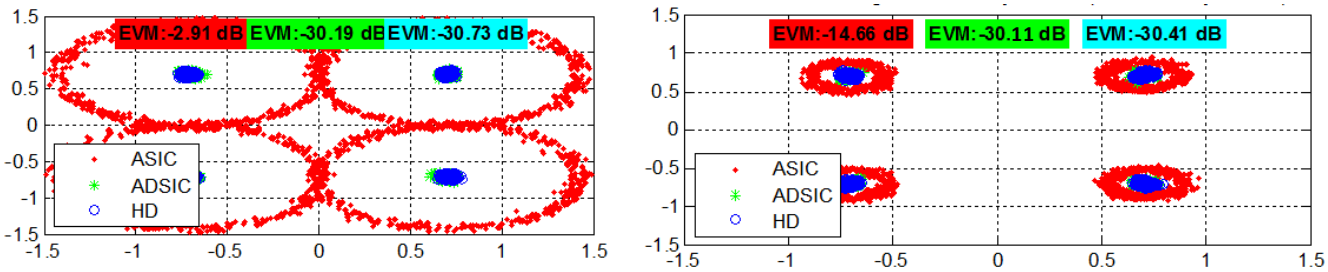


FIGURE 59. Impact of analog self-interference cancellation on FD wireless link performance (QPSK digital modulation scheme).



(A) (B)

FIGURE 60. Received constellation diagrams for different amounts of analog SIC. (A) 40 dB of analog SIC, B) 60 dB of analog SIC.

Using only analog self-interference cancellation results in a limited performance of the wireless link. The EVM is -15dB for 60 dB of analog SIC, while the EVM of the half-duplex link is around to -31 dB. However, as already described, the digital cancellation block reduces the self-interference up to the receiver noise floor, which improves the full-duplex reception performance up to the half-duplex received EVM, as FIGURE 61 shows. This improvement can be visualized also in FIGURE 60(A) and FIGURE 60(B). The green points represent the constellation diagrams and EVM for the full-duplex link (including analog and digital cancellation), while the blue points correspond to the half-duplex link. As can be seen from the obtained results, minor degradation is obtained for the full-duplex transmission.

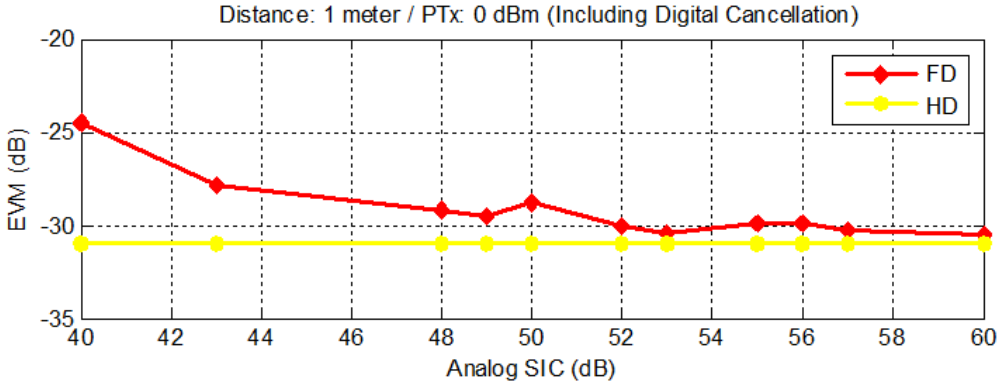


FIGURE 61. EVM performance including digital cancellation for different values of analog cancellation.

4.2.2.2. *Performance evaluation over link distance*

The full-duplex link performance has been evaluated over different link distances. FIGURE 62 illustrates the EVM performance during full-duplex operation versus the link distance for different modulation schemes up to 64QAM. Both local and remote nodes are transmitting 0 dBm (measured at the output of the WARP) and they provide an analog SIC of 60 dB in 20 MHz BW. FIGURE 62 shows the EVM performance at the local node, when only analog cancellation is applied (FDAC), when both analog and digital cancellation are applied to reduce SI (FDADC) and when the nodes operate in half-duplex (HD), i.e. when not transmitting any data simultaneously. The performance achieved at both nodes when both transceivers have the same analog cancellation and transmit the same power is similar, except for minor deviations (<3dB in the EVM performance). These deviations can be caused by differences in the hardware, e.g. different antenna gain at both nodes. Therefore only the performance of one of the nodes is shown in this section.

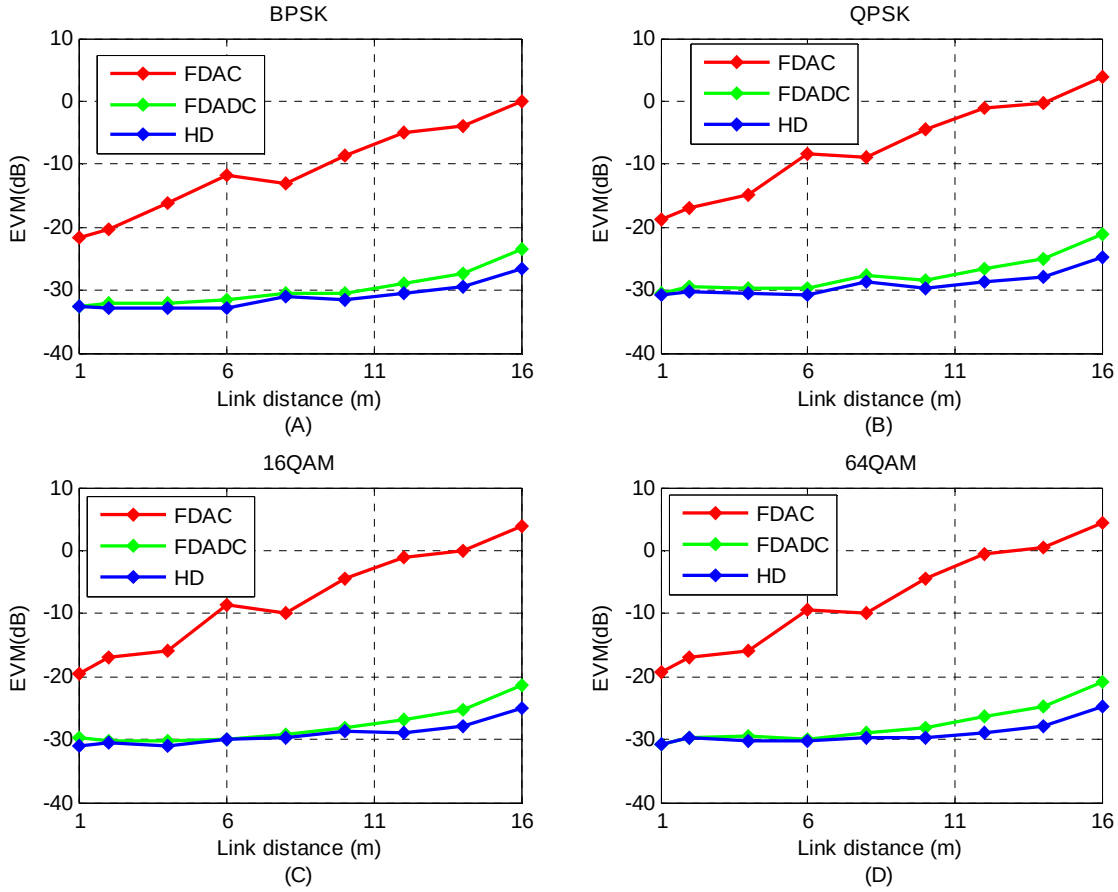


FIGURE 62. EVM performance over link distance for different modulation schemes. (A) BPSK, (B) QPSK, (C) 16QAM, (D) 64QAM. Transmit power at local and remote node is 0 dBm.

It is observed that full-duplex mode achieves similar performance to half-duplex for distances shorter than 10 meters. For distances larger than 10 meters, the difference between FD and HD EVM starts to increase up to 2% at the maximum link distance of 16 meters, as FIGURE 63 illustrates.

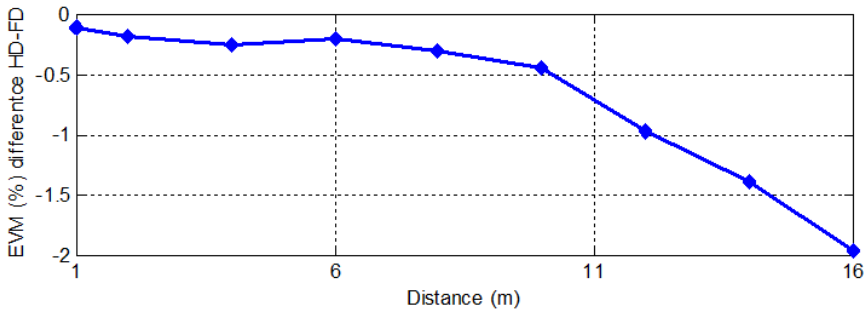


FIGURE 63. FD and HD performance comparison.

The increase in the PTX at the local node will improve the EVM at the remote node. However, the EVM of the local node will be degraded due to the SI if the power transmitted by the remote node is the same. In this case, the power of the received signal at the local node is the same but the self-interference signal is larger and the FD performance is degraded (the digital cancellation does not cancel the total SI and there is an increment in the receiver noise floor), as FIGURE 64 shows. In this scenario, the difference between the FD and HD EVM performance is larger than 15%. The issue of the transmit power is addressed also in section 4.2.2.3.

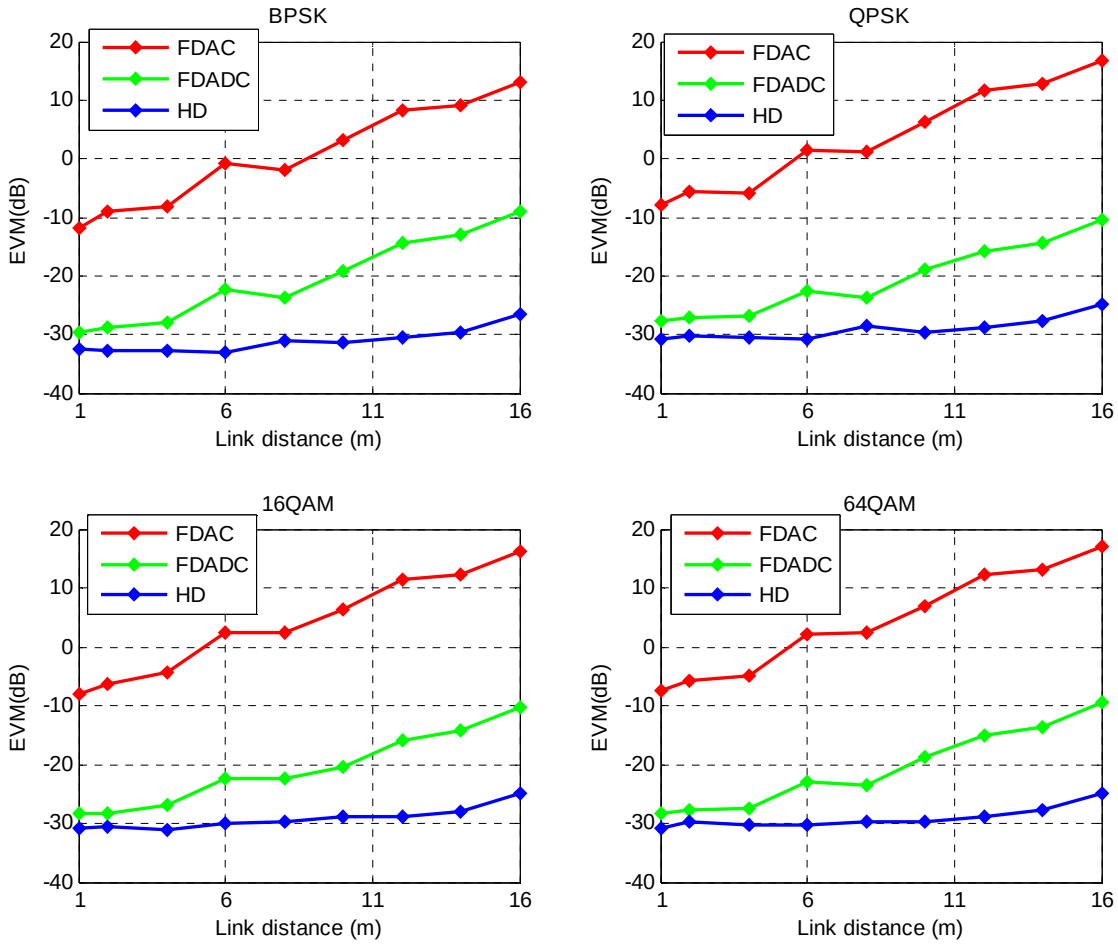
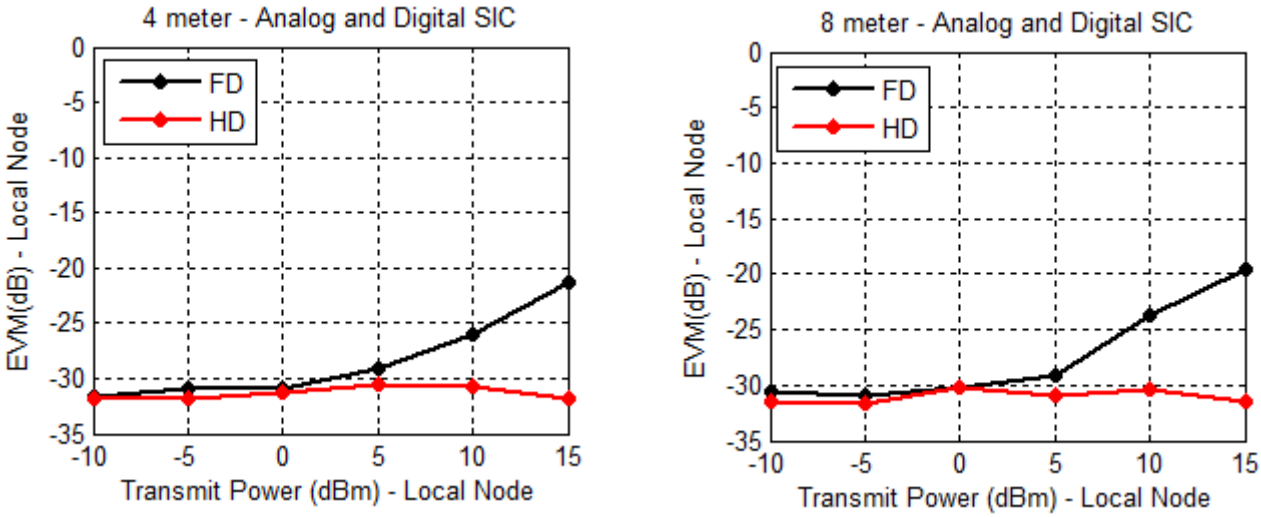


FIGURE 64. EVM performance over link distance for different modulation schemes. (A) BPSK, (B) QPSK, (C) 16QAM, (D) 64QAM. Transmit power at local is 15 dBm, transmit power at remote node is 0 dBm.

4.2.2.3. *Transmit Power*

As already described in this document, the transmit power can improve the signal-to-noise ratio at the receiver resulting in a better EVM figure. However, this happens only in the case of the half-duplex operation. In the case of FD, the transmit power causes the increase of the self-interference, degrading the reception performance.

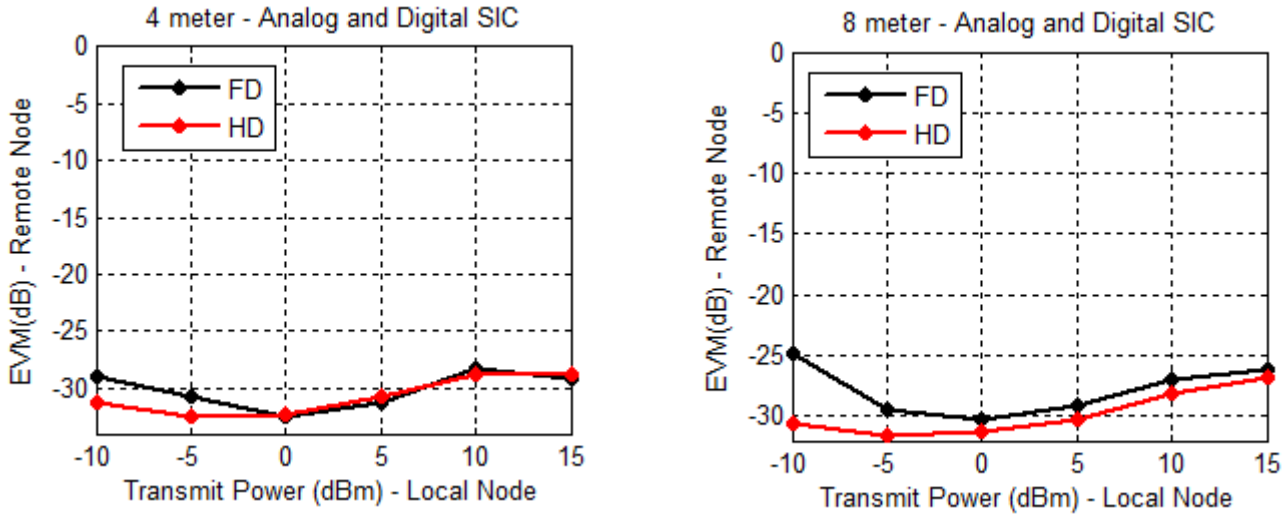
FIGURE 65 shows the relation between the EVM performance at the local node and the transmit power, when only the PTX at the local node is modified and a 64QAM modulated signal is transmitted. In HD operation the EVM remains the same due to the transmit power at the remote node does not vary, thus the power of the received signal at the local node is the same. However, in FD transmission, the higher the transmit power, the worse the EVM performance. This is due to the increment in the receiver noise floor due to the SI. Considering that the receiver noise floor of the WARP is around -85 dBm and the SIC of the dual-port antenna demonstrator is 90dB, this means that the receiver noise floor will be increased when the PTX power is larger than 5 dBm, as FIGURE 65(A) and FIGURE 65(B) illustrate. The degradation is deeper when the link distance is larger due to the received signal of interest is smaller because of the propagation losses, as FIGURE 65(B) shows. (This issue will be addressed also in section 4.2.2.5).



(A) (B)

FIGURE 65. EVM at the local node versus the transmit power of the local node. (A) Link distance: 4 meters, (B) Link distance: 8 meters.

Additionally, FIGURE 66(A) and FIGURE 66(B) shows the EVM measured at the remote node versus the PTX at the local node, when the nodes are separated 4 meters and 8 meters respectively. As can be seen from the obtained results, the increment of the PTX at the local node improves the EVM of the remote node in both HD and FD transmissions, although a small degradation is observed at PTX larger than 10 dBm caused by the non linearities introduced by the transmitter at these high transmit powers.



(A) (B)

FIGURE 66. EVM at the remote node versus the transmit power of the local node. (A) Link distance: 4 meters, (B) Link distance: 8 meters.

4.2.2.4. *Symbol error rate*

FIGURE 67(A) shows the measured symbol error rate versus the link distances for different modulation schemes up to 64QAM when the self-interference is cancelled below the receiver noise floor. As can be seen from the obtained results, error-free digital data reception over a link distance of 10 meters is achieved for BPSK, QPSK, 16QAM and 64QAM modulation schemes. At the maximum distance of 16 meters, the symbol error rate is below 10^{-2} for the 64QAM modulation scheme.

Additionally, the effect of increasing the transmit power in the local node (maintaining the same transmit power in the remote node) has been also analyzed. FIGURE 67(B) illustrates the symbol error rate versus the link distances for different modulation schemes when the transmit power is higher and there is an increment in the receiver noise floor due to the self-interference (while the strength of the received signal is the same). The self-interference after digital cancellation is approximately 10 dB above the receiver noise floor. As can be observed, the symbol error rate degrades because of the self-interference. For a 64QAM modulation, the symbol error rate is 0.3 at the maximum distance of 16 meters. For BPSK and QPSK modulation schemes, there is still error-free data reception over a link distance of 10 meters.

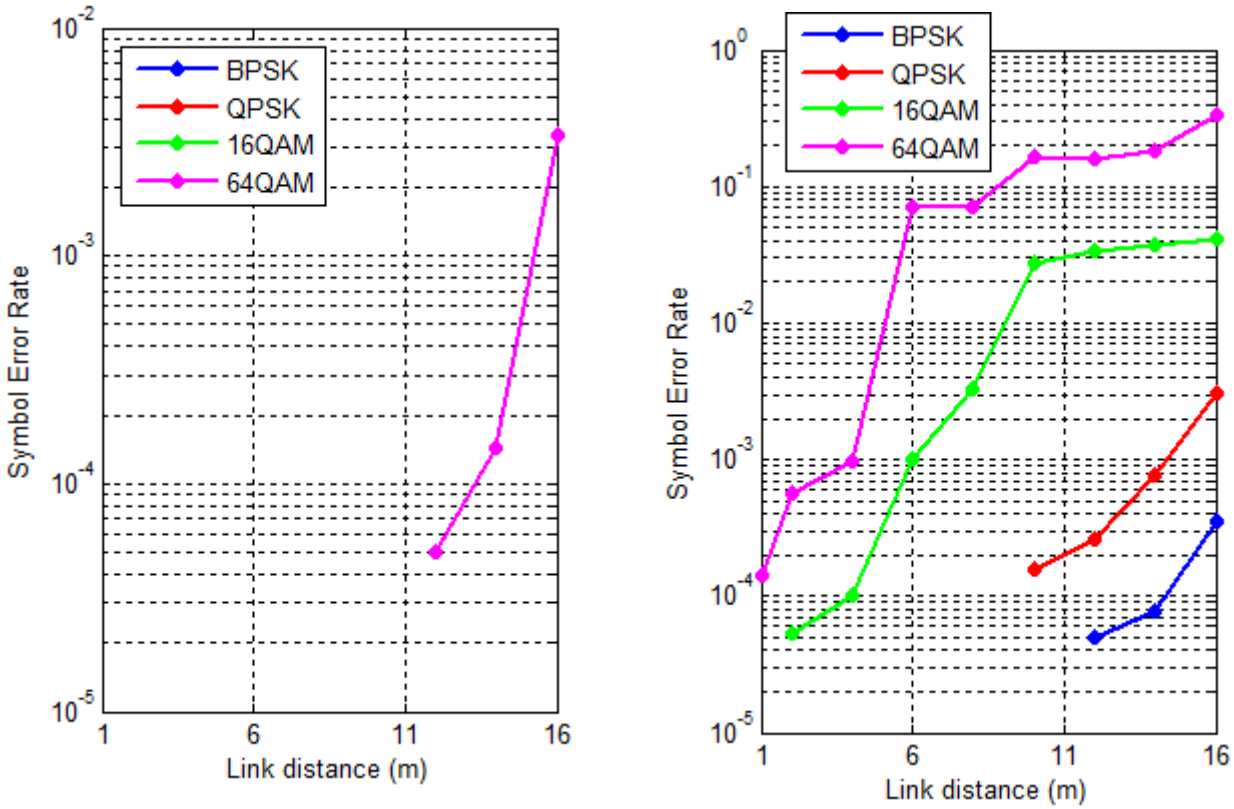
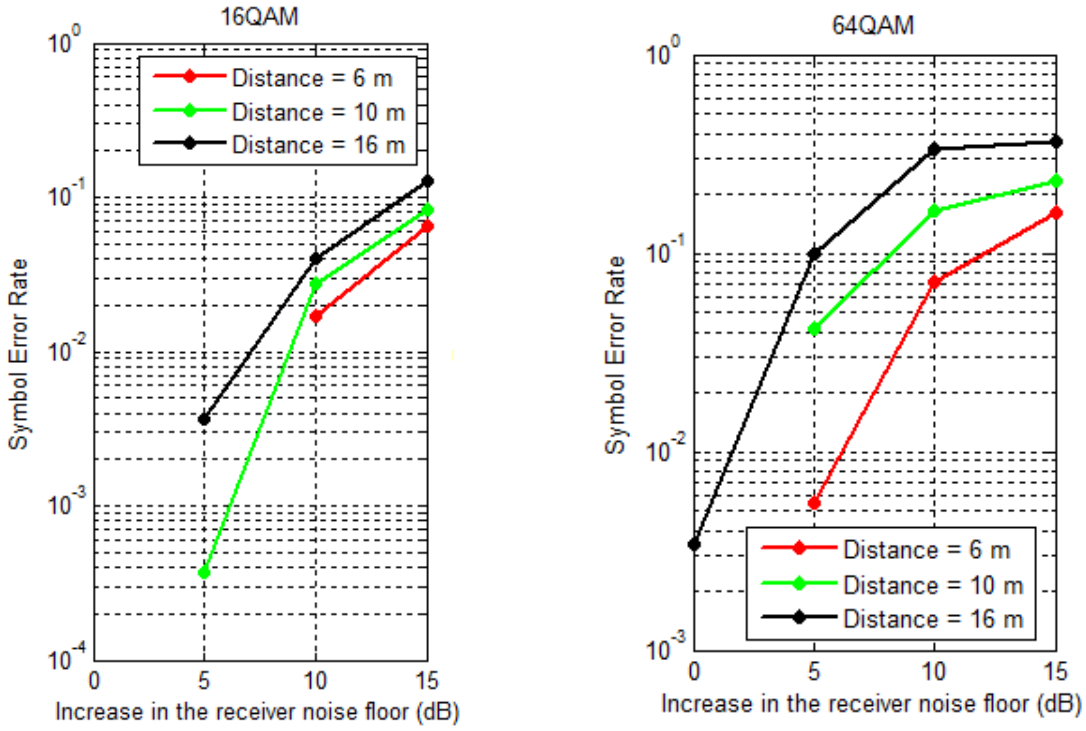


FIGURE 67. Symbol error rate versus the link distance. (A)there is no increment in the receiver noise floor, (B) the increment in the receiver noise floor is 10 dB.

FIGURE 68(A) and FIGURE 68(B) depict the symbol error rate versus the increase in the receiver noise floor for a 16QAM and 64QAM modulated signal. As can be seen from the obtained results, the increment in the receiver noise floor due to the self-interference causes the symbol errors in the received signal. This effect is stronger when the link distance increases, i.e. when the received signal strength is lower due to the propagation losses.



(A) (B)

FIGURE 68. Symbol error rate versus the increase in the receiver noise floor. (A) 16QAM, (B) 64QAM

4.2.2.5. *Digital cancellation versus analog cancellation*

As already reported in this document, the digital cancellation algorithms cancel the self-interference signal that still remains after the analog cancellation block. This digital cancellation block increases in around 30 dB the cancellation provided by the active cancellation network and the dual-polarized antenna. However, the performance of the digital cancellation block depends, to some extent, on the analog cancellation level. FIGURE 69 illustrates the digital cancellation versus the analog cancellation performance. As can be seen from the obtained results, the increase of SI cancellation at analog level reduces the performance of the digital cancellation. Additionally, the obtained results show how the digital cancellation implemented in the DUPLO demonstrator presents and upper limit around 34 dB. This fact can diminish the full-duplex link performance when the analog cancellation is reduced, and it provokes also that the self-interference is not completely removed when high TX powers are used, as section 4.2.2.3 describes. This increment in the receiver noise floor will result on a reduction of the full-duplex link range, as already described in section 4.2.2.4.

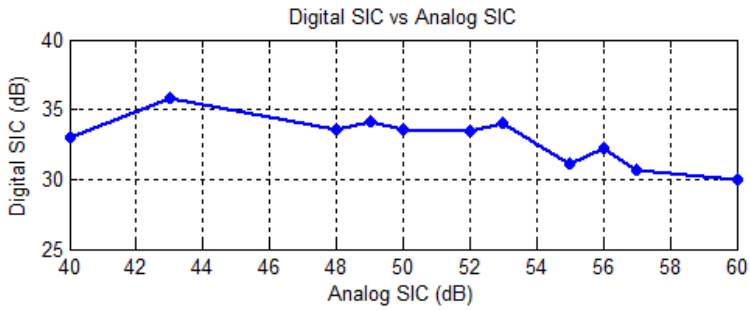


FIGURE 69. Digital cancellation performance versus analog cancellation performance.

5. ANALYSIS OF THE RESULTS AND FUTURE OPPORTUNITIES

Section 4 reports the results obtained from the validation of the DUPLO demonstrators under different scenarios and operating conditions. Now, this section gives an overview of the main findings gained from the testing stage of the DUPLO radio transceivers.

With regard to the single port antenna demonstrator, the main takeaways obtained from the measurements are:

- The measurements quantify the communication performance over a wireless link between two full-duplex nodes, where these nodes implement the first version of the DUPLO electrical balance duplexer in combination with a commercial single port antenna
- If the antenna impedance is in the tuning range of the balance network, the RF SIC exceeds 48 dB
- The digital SIC improves the RF SIC with about 17 dB
- The coverable link distance rages up to 1 meter
- The preferred transmit power is 0 dBm
- Over a normal link distance of 60 to 80 cm's, a FD EVM around -17 dB is achieved
- Experiments have been performed over a 20MHz bandwidth; a smaller bandwidth show an increase of the maximal RF SIC (cancelling the transmitter induced SI)
- Error-free digital data reception over a link distance of 60 cm is achieved for BPSK, QPSK and partially for QAM16

Several of the performance limiters are caused by known issues, such as the limited linearity of the balance network and the narrow bandwidth characteristics of the R/C balance network. These issues have been tackled in [3] by a new balance network design, but to maintain the project timeline it was agreed that this second prototype was not included in WP5.

With regard to the dual-port antenna demonstrator, the main conclusions obtained from the testing stage are:

- The dual-polarized antenna provides a self-interference isolation of 50 dB in the overall signal bandwidth, however this isolation is really sensitive to the changes in the environment. Measurement results show how the self-interference suppression can decrease in more than 8 dB when metallic objects are place close to the antenna.
- The active cancellation network reduces the negative effects of the objects close to the antenna maintaining the analog self-interference cancellation above 50 dB. For normal operation of the antenna, i.e. 50 dB of self-interference isolation, the active cancellation network increases the SIC up to 60 dB in 20 MHz BW.
- The digital cancellation block improves the analog SIC with about 30 dB. The digital cancellation algorithm implemented in DUPLO project presents an upper limit of cancellation of around 34 dB. This reduces the performance of the full-duplex transceiver when high TX powers are used. This is due to the presence of self-interference after digital cancellation, and therefore the increase in the receiver noise floor. As expected, the degradation of the FD performance is higher for larger link distances.
- The full-duplex performance in terms of EVM is comparable with half-duplex performance for distances up to 16 meters (when the SI is reduced till the receiver noise floor). Only a minor degradation of about 2% is observed for the full-duplex transmission mode.
- The preferred transmit power is 0 dBm. The wireless link distance does not improve for higher transmit powers. On the contrary, the performance of the full-duplex transmission is decreased due to the self-interference.

- Error-free digital data reception over a link distance of 10 meters is achieved for BPSK, QPSK, 16QAM and 64QAM, when the self-interference is completely reduced below the receiver noise floor.
- The degradation of the analog self-interference increases the symbol error rate of the FD communication. This is due to the limitation presented by the digital cancellation algorithms which is around 34 dB of SIC.
- Better performance in terms of cancellation bandwidth could be achieved if analog delay lines are included in the active cancellation network. However, this increases the size of the analog circuitries and also the complexity of the automatic tuning algorithms.

The results obtained from the validation of DUPLO proof-of-concept have demonstrated the feasibility of the implemented solutions in full-duplex applications. On one hand, the single-port antenna demonstrator enables full-duplex operation in portable system radio devices. This full-duplex transceiver provides high integration potential for short range or narrow bandwidth FD communication applications. On the other hand, the dual-port antenna demonstrator enables full-duplex communication in compact form-factors providing full-duplex operation over larger coverable link distances. The main limitations presented by the implemented solutions are due to the limited bandwidth of the analog solutions and the limited linearity. However, these issues can be tackled by new designs of the analog solutions as described in [3].

The work developed within DUPLO project mainly differentiates with the state-of-art in terms of form factor and integration potential in compact radio devices. TABLE 5 depicts an overview of the recent works on full-duplex transceivers. As can be seen from the listed references, most of the proposed solutions [18]-[21] rely on the use of separate antennas for transmission and reception. This increases the self-interference isolation between transmitter and receiver but hampers the integration in compact radio devices. However, both DUPLO demonstrators integrate a single antenna solution that enables full-duplex operation with good analog self-interference cancellation performance. The full-duplex radio transceiver published in [22] makes use of a single antenna with a single port connected to a circulator. Additionally, this radio node uses an analog cancellation network with multiple analog delay lines to mimic the self-interference channel. This FD transceiver achieves good performance in terms of cancellation bandwidth, although again, its integration is compact form factor is really critical due primarily to the circulator and analog delay lines.

Apart from the advantages in terms of form-factor provided by DUPLO demonstrator, the performance offered by both DUPLO demonstrators allows full-duplex operation over different link distances. As already presented in this document, 66 dB and 90 dB of self-interference cancellation is achieved over 20 MHz BW for the single-port and dual-port antenna demonstrator respectively. According to this numbers, only the works presented in [18] and in [22] could improve this performance. As already mentioned, the radio transceiver reported in [22] is rather difficult to scale towards a compact form-factor due to the analog delay lines included in its cancellation circuitry. Similarly, the full-duplex radio node developed in [18] is not compatible with compact radio devices because of it uses two separate directive antennas to achieve large self-interference suppression at antenna level.

TABLE 5. State-of-the-art overview of full-duplex demonstrators.

Reference	Description of the FD demonstrator	Self-Interference Cancellation	Bandwidth
[18]	Separate antennas for transmission and reception (50 cm distance), optional use of cross-polarized antennas. Active RF and BB cancellation	95 dB	20 MHz
[19]	Two antenna solution and balun cancellation complemented with digital cancellation block	73 dB	10 MHz
[20]	Pair wise Triple-wise, symmetrical antennas. Active cancellation based on corrective beam-forming with auxiliary transmitted signal recovery at base-band	70 dB	Not specified
[21]	Separate antennas for transmission and reception (20cm distance) RF cancellation with additional RF chain Digital BB interference cancellation	78 dB	625 KHz
[22]	Single antenna solution with circulator. Analog cancellation implemented by means of dynamic adaptation of delays + attenuators (60 dB). Digital cancellation (50 dB)	110 dB	80 MHz

The self-interference cancellation solutions developed in DUPLO project provide adaptability to the changes in the environment through the automatic tuning of the analog cancellation solutions. This ensures the full-duplex operation over a wide range of operating conditions, as reported in this document. Furthermore, the results obtained from DUPLO demonstrator validation and testing indicate that in short transmission distances, the impact of self-interference can be reduced up to the level where the signal reception quality is not compromised, achieving similar performance to half-duplex mode.

These promising results confirm the benefits of full-duplex technology related to spectral efficiency at physical layer. Moreover, full-duplex concepts can be advantageously utilized in higher layers, such as at the access layer by reducing the air interface delays and facilitating improved collision detection/avoidance mechanism in contention based networks. Taking this into account, full-duplex technology can be considered as a great point of interest for future 5G systems.

6. SUMMARY AND CONCLUSIONS

This document describes the final integration and validation of the DUPLO proof-of-concept. Two DUPLO demonstrators have been implemented targeting two different compact form-factors. The first demonstrator (single-port antenna demonstrator) enables full-duplex operation in ultra small radio devices such as smartphones or smartwatches. The second implemented demonstrator (dual-port antenna demonstrator) targets compact radio devices such as small cell access points.

DUPLO project has identified small cells as one of the main areas of interest for the project, mainly because of small areas with short link distances and low transmission powers is the preferred scenario for full-duplex technology development. Considering this scenario, full-duplex transmission can provide system level performance gains over half-duplex with a self-interference cancellation level of 70-90 dB. To satisfy this requirement in terms of self-interference mitigation, DUPLO demonstrator implements different analog and digital self-interference cancellation techniques at different stages of the full-duplex transceiver. The analog cancellation solutions have been developed in DUPLO WP2 and provide good performance in terms of self-interference cancellation in small form-factor. The digital cancellation algorithms have been investigated in DUPLO WP3 and cancel the self-interference that remains after the analog cancellation stage.

The single-port antenna demonstrator consists of an electrical balance duplexer processed in plain CMOS technology and a single-port PIFA antenna. The balance networks adapts to the antenna impedance over different operating conditions in order to achieve self-interference suppression from the transmitter to the receiver. Two different automatic tuning algorithms have been implemented for the EBD in order to dynamically adapt to the changes in the antenna impedance. The first algorithm is based on conventional binary search tree, while the second algorithm is more advance and exploits specific characteristics of the EBD. This second algorithm is executed in two phases. The first phase is the training and modelling phase during which the algorithm is trained to characterize the effect of digitally controlling the balance network on the SIC. During the second phase, the tuning is performed during system operation using the measured SIC value to estimate the difference between the EBD and antenna impedance and find the R/C code which minimize this difference. Both algorithms have been developed to maintain the normal transmit operation during tuning, reduce the overhead and to preserve the digital design complexity, as section 3.1 describes.

The dual-port antenna demonstrator is integrated by a dual-polarized antenna with two excitation ports implemented in microstrip technology. This antenna operates with orthogonal polarizations in transmission and in reception to achieve self-interference isolation at antenna level. Additionally, the dual-polarized antenna is combined with an active cancellation network to compensate the effects of nearby objects close to the antenna which can degrade the antenna isolation. The cancellation network works at analog RF frequencies. It takes a copy of the TX signal and applies a variable attenuation and a variable phase rotation. Then the cancellation network combines this attenuated and phase-shifted copy of the TX signal with the self-interference that leaks from the antenna. The active cancellation network includes a self-interference detector to find the attenuation and phase shift coefficients that minimize the self-interference after the active cancellation by means of using a gradient descent algorithm. The algorithm can dynamically adapt the attenuation/phase coefficients to the changes in the environment, maintaining the analog SIC above a predefined threshold for a wide range of operational conditions. The active cancellation network has been implemented in a PCB using off-the-shelf components. In addition, the STM32F4 microcontroller has been used to set the analog control voltages of the attenuator and phase shifter and to run the gradient descent algorithm, as section 3.2 reports.

As abovementioned, both DUPLO demonstrators include a digital cancellation algorithm to cancel the remaining self-interference signal. This digital cancellation has been implemented in MATLAB as a feed forward filter. Two different digital baseband SIC methods are used depending on the time synchronization of the received and self-interference signals. If SI and received signal are time synchronized, then frequency domain cancellation gives the best performance while time domain cancellation provides better results when signals are not time aligned. The digital cancellation block forms part of the full-duplex baseband developed

for the DUPLO project. This FD baseband has been also developed in MATLAB and it consists of an OFDM based waveform with sixty four subcarriers, as section 3.3 presents.

Both developed demonstrators have been integrated using WARPv3 radio board and WARPLab 7.4 framework. WARPLab framework enables PHY prototyping using WARP hardware for waveform transmission/reception and MATLAB for signal processing. By doing so, the arbitrary I/Q signals samples generated in MATLAB are sent to the WARP board via the Ethernet cable to their up-conversion and transmission. Likewise, the signals received by the WARP board are down-converted and transferred to the MATLAB for post-processing. The two RF interfaces of the WARPv3 are used; one of these interfaces is configured as transmitter and the other as the receiver. WARP is using channels in the 2.4 GHz ISM band with a signal bandwidth of 20 MHz.

Both demonstrators have been validated under different operational conditions and a full-duplex wireless link has been demonstrated, as section 4 reports. With regard to the single-port antenna demonstrator, the self-interference cancellation provided by the overall transceiver is around 70 dB in 20 MHz bandwidth (17 dB provided by digital cancellation). A full-duplex wireless link with two single-port antenna radio nodes has been evaluated for link distances up to 1 meter using different transmit powers and modulation schemes. Over normal link distances of 60 to 80 cm's, a FD EVM around -17 dB is achieved and the FD performance is similar to the HD mode. Furthermore, error-free digital data reception over a link distance of 60 cm is achieved for BPSK, QPSK and partially for 16QAM. With regard to the dual-port antenna demonstrator, the SIC provided by the FD transceiver is around 90 dB in 20 MHz BW, 30 dB of which are provided by the digital cancellation. The full-duplex performance achieved with this radio transceiver is comparable with half-duplex performance for distances up to 16 meters with a minor degradation of about 2% in the EVM of both transmission modes. Moreover, error-free digital data reception over a link distance of 10 meters is achieved for BPSK, QPSK, 16 QAM and 64 QAM, when the self-interference is completely reduced below the receiver noise floor. However, a degradation of the full-duplex performance is observed when high transmit powers are used, i.e. PTX> 5 dBm, due to the presence of self-interference after the digital cancellation.

The main limitations of the proposed solutions are related with the limited linearity and the narrow bandwidth of the analog solutions. However, some of these issues have been already tackled in DUPLO project, as deliverable D2.2 [3] describes. This opens the door to future opportunities towards the improvement of the proposed solutions.

The results obtained from the validation of DUPLO proof-of-concept have demonstrated the feasibility of the implemented solutions in full-duplex applications. Both DUPLO demonstrators enable full-duplex operation in compact commercially attractive radio devices, being the small form factor one of the key differentiators from the state-of-the-art. These promising results confirm the benefits of full-duplex technology related to spectral efficiency at physical layer and pave path for introducing the full-duplex technology in the future 5Gnetworks.

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