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for Space Applications and Research

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Final Public Report

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SEVENTH FRAMEWORK PROGRAMME

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1 Introduction

The European Project CESAR-SPACE ended in May 31st this year. It was not obvious, in a daily rhythm, to appreciate the work done in three years. Most of the time, we are facing objectives, budgets and schedules and seeking for reports from our colleagues to finish our own reports, all this in the side of our institutions duties. When filling the final document we have a better view of all the work done in a relatively short period for the kind of application: cryogenics is always a good occasion to experience patience and modesty.

When performing measurements at very low temperature, 4K or under, a wide distance is set between the experimentalists and the experiment. They generally have to pump the cryostat where your setup is located; this means that all the vacuum leakages are already fixed. Cooling down and warming up is also a very time-consuming process especially when you realize that a wire (essential of course) broke during these operations.

For obvious thermal budgets constraints, experimentalists reduce as much as possible the links between warm temperature (where we live) and the purpose of the experiment. The links are then fragile, subject to vibration easily perturbed, things that look paradoxical with the goals of the experiments: obtain small noise levels and high gains.

The objectives have been fulfilled: we are now able to measure cryogenic electronic devices manufactured during the CESAR process, not only at the elementary component level, but also at the circuit level. All the measurements are not positive. Many reasons for that: Nature at the fundamental level is most of the time different from the way we think it. The logical consequence is that experiments are not supposed to work, except when you develop a step-to-step strategy to overcome all the possibilities to fail. Sometimes a surprise can occur. In science we call that serendipity. This was the case during the GeJFET development. It is not yet guaranteed that we can produce this kind of component in a well-defined and reproducible process, but the way to realize “clean” electrical contacts in Ge or other transistor types is now straightforward. The very high doping level contact obtained by laser pulses is now well established.

The quest for HEMTs with very high noise quality working at very low temperature was a long quest in many labs around the world. Thanks to the CESAR program, due to the internal visibility given by this type of European Grant at the institutional level, the program could be achieved. These HEMTs were later incorporated to more fields of the CESAR development (Magnetometry) than initially planned. The LPN HEMTs were, outside the CESAR program, widely distributed in most of the preeminent Dark matter experiments (CDMS, EDELWEISS,…).

At the semi complex level, the CMOS ADC chips gave excellent results very soon in the CESAR development. Some failures on other chips have the manufacture of complex circuits. This gave time to built and test efficiently the setup for the defined applications: X-Ray Calorimetry, Far Infrared Photometry and space magnetometry.

2 Elementary Components (WP2)

Objectives

« Design, fabricate and supply various cryogenic Ge, SiGe and AsGa based transistors for front end readout electronics at T ≤ 4.2 K and to push their performance better than that of the current Si JFETs at T > 100 K in terms of the low frequency noise, input capacitance and power consumption. »

2.1 HEMTS

Progress toward objectives

HEMTs: During the third year of the project, experimental results show that cryogenic HEMTs made at LPN for low-frequency and low-temperature can replace silicon JFETs at a temperature below 77K (the operating temperature of silicon JFETs is limited at T>100K). Under the same input capacitance condition (HEMT versus JFET), the input noise-voltage of cryogenic HEMTs at 4.2K by this project can be as low as or even better than that obtained by silicon JFETs at T>100K. Beyond the noise voltage, noise currents from these HEMTs at 4.2K show an unprecedented low value from a few tens of aA/Hz½ to a few aA/Hz½ at 1Hz, according to the input capacitance. **Therefore, we have achieved a breakthrough in realizing high performance cryogenic electronics and fulfilled our initial objectives**.

In addition of the objectives by this project for space cryogenic electronics, our HEMTs have been used in the mesoscopic physics for the measurement of quantum limit of heat flow across a single electronic channel (see *Science* **342**, 601 (2013)). These HEMTs have also been selected and the CNRS/LPN has been elected as a member for cryogenic dark matter search experiences in Europe (see http://edelweiss2.in2p3.fr/Collaboration/index.php) and in US (see http://cdms.berkeley.edu/cdms_collab.html).

Significant results

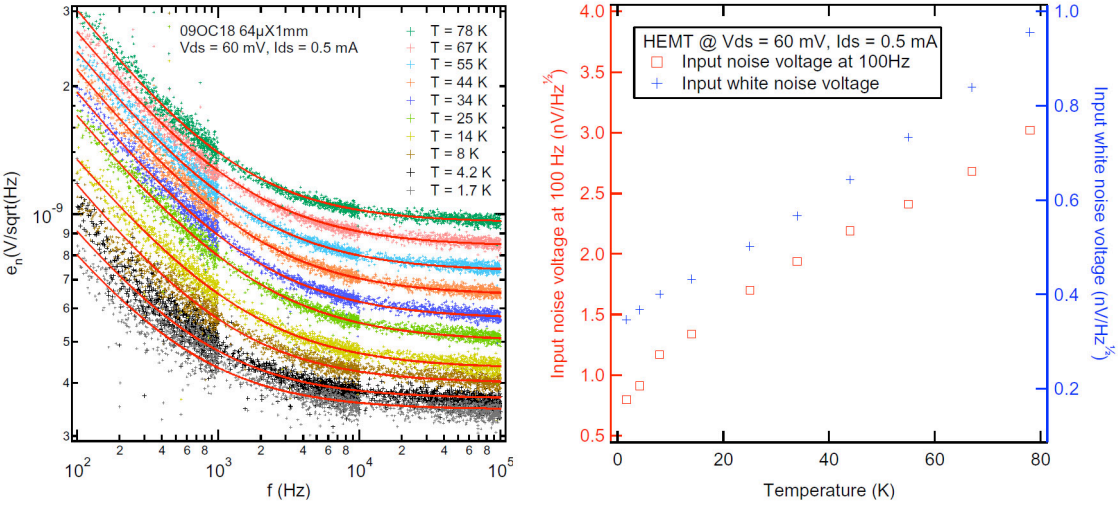
- A breakthrough on the low-frequency noise performance for the HEMTs at 4.2 K has been accomplished: their noise voltage can be lower than the records held by silicon JFETs at T>100K since decades, few nV/Hz½ at 1Hz and well below 1nV/Hz½ at 1kΩ. The lowest noise voltage, i.e., the white noise voltage can be very close to 0.1nV/Hz½; in particular the noise current in the HEMTs at 4.2 K can be unprecedented low in the range of aA/ Hz½ at 1Hz.

- The power consumption for these HEMTs can be limited below 100µW down to 1nW depending on the amplifier specifications.

- The operating-temperature range for cryogenic HEMTs by this project is below 77K, there is no low temperatures limit. Noise measurements have been performed from 77K down to 1,7K. For all noise parameters, the lower the temperature, the lower the noise values can be obtained.

- Temperature dependence of the noise voltage

In the two figures below, we report experimental observations of the temperature dependence of the input noise voltage from 77K down to 1.7K obtained from a cryogenic HEMT. The left shows the noise spectra as function of the temperature. The right shows the evolution of the white noise and low-frequency noise at 100Hz as function of the temperature. General remark is that noise values increase with the increase of the temperature.



From the above right figure we can find, with the increase of the temperature of more than 40 times:

- the white noise increases less than 3 times;

- the low-frequency noise at 100Hz increases of about 4 times.

The same characteristics have been observed in different cryogenic HEMTs, therefore the lower the operation temperature, the better the performance of these HEMTs will be.

In the future, we will continue to optimize the material growth, design and fabrication process in order to realize a white noise below 0.1nV/Hz½ and a better understanding of the 1/f noise in the field-effect transistors. Finally to attain the 1/f noise limit in cryogenic HEMTs.

2.2 CSNSM final activity report for CESAR

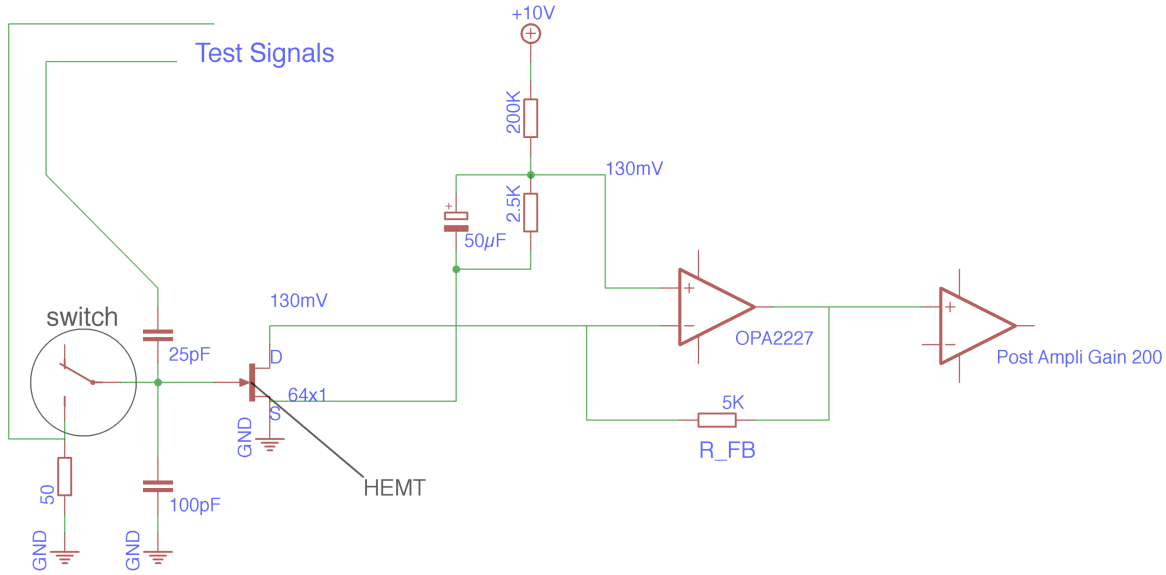
2.2.1 Introduction

In the framework of the CESAR project the CSNSM-CNRS laboratory has tested the performances of cryogenic charge amplifiers using HEMT frond-end transistors. The HEMT components where manufactured at LPN and specifically optimized for low temperature operation and very low voltage, current and 1/f noise. Several cryogenic configurations have been tested, either connecting the HEMT gate with a test capacitance and resistor or with a specifically designed cryogenic Germanium detector.
HEMT performances and figure of merit are compared with state of the art JFET-based amplifiers. HEMT cryogenic amplifiers are very promising for a variety of low temperature detection experiments, in the domain of Astrophysics and observational Cosmology. Improving

the low frequency noise (0-10kHz) is particularly critical for these applications since it provides lower energy thresholds and enhanced energy resolution.
During the last year of the CESAR project we have studied two specific setups with HEMT based front-end electronics cooled down to 4.2K. We summarize in the following sections our results.

2.2.2 First setup : HEMT biased at constant voltage (V_s=GDN, V_{ds}=cte)

In this setup the HEMT is used in a current amplifier mode. It transforms a voltage signal on its gate DV_{gs} $(D(V_{gate}\text{-}V_{source}))$ to a current variation Di_{ds}, which is post-amplified at 300K. The source of the HEMT is connected to the ground at the 4.2K stage of the cryostat. The 300K current post-amplifier fix the drain voltage of the HEMT at a constant value. The drain-source voltage of the HEMT is equal to 130mV, corresponding to the saturation regime of the transistor.



In this configuration the gain of the transistor is given by its trans-impedance $g_m = {d(i_{ds})}/{d(V_{gs})}$. This latter depends on the operating point of the HEMT (V_{gs}, V_{ds} and i_{ds}).
To measure g_m, a calibated AC voltage (in the form of pulses) is applied to the gate, that is switched to the 50Ω resistance. To measure the input capacitance (C_{gs}+C_{ds}) of the HEMT, the gate is switched-off the 50Ω to the capacitive 100pF configuration, and a test signal is sent to the 25pF capacitance. The test voltage DV_{test} induces a signal on the gate DV_g equal to:

$$\Delta\left(V_{test} - V_g\right) \cdot C_{test} = \Delta V_g \cdot \left(C_{HEMT} + 100pF\right)$$

$$\Rightarrow C_{HEMT} = \left(\frac{\Delta V_{test}}{\Delta V_g} - 1\right) \cdot C_{test} - 100pF$$

Two HEMTs have been tested showing an input capacitance C_{HEMT} = 200pF. The total gain of the setup is given by the equation : $G = g_m \times R_{FB} \times G_{PostAmpli}$
R_{FB} is the feedback resistance of the OPA2227 operational amplifier (5KΩ in our case), and $G_{PostAmpli}$ = 200 is the gain of the post-amplification stage.
A summary of our measurements is given in the table below.

	V_{ds}	I_{ds}	*Total gain*	g_m	C_{HEMT}
HEMT t3	132 mV	1.1 mA	24000	24 mS	200pF
HEMT t4	132 mV	1.7 mA	36000	36 mS	200pF

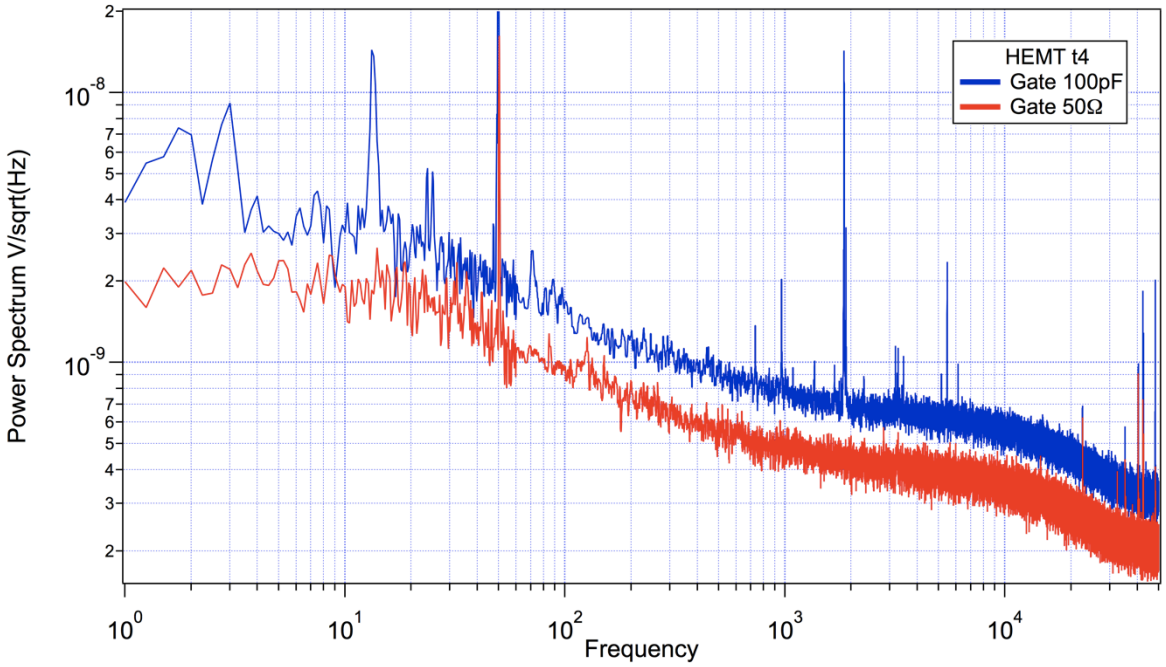
In the case of a Ge detector the HEMT will be configured as a charge amplifier. The voltage induced in the gate by the charge signal Q is given by the following equation:

$$Signal = \Delta V_{gs} = Q/(C_g + C_{HEMT})$$

with $C_g = C_{detector} + C_{cabling}$

The signal to noise ratio is given by the equation : $\frac{Signal}{Noise} = \frac{Q}{e_n \cdot (C_g + C_{HEMT})}$

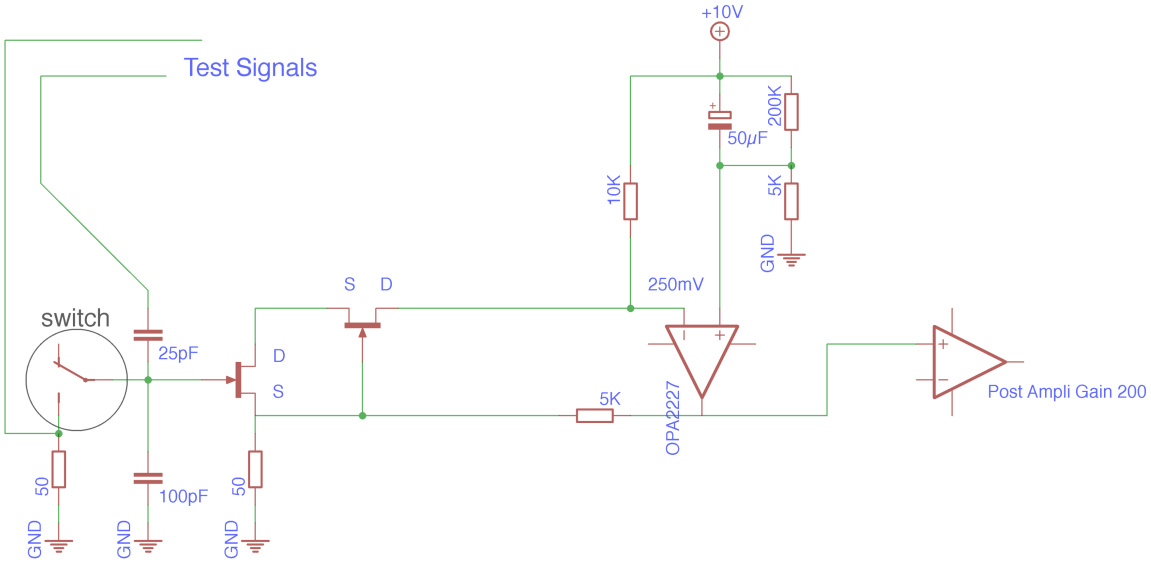
The measured noise spectra in the high impedance and low impedance case (50Ω or 100pF) are given below.



We observe a clear 1/F behavior that is caracteristic of all HEMT components. The overall noise is very low, comparable to state of the art JFET based amplifiers. We measure a difference of 1.5 over the entire frequency range in the noise spectrum between the two gate setups (50Ω and 100pF) which is not yet well undestood. This difference is not observed in the second setup described hereafter.

2.3 Second setup: voltage amplifier with compensated Miller effect

In this setup the HEMT is used in a voltage amplifier configuration. The gain is given by the ratio between the 5kΩ and 50Ω resistors connected at the source of the transistor. The HEMT is biased at constant current I_{ds}, controlled by the operational amplifier OPA2227 and adjusted by the *10k*Ω resistor (I_{ds} = *10V/10k*Ω = 1mA in the following case).



For a HEMT biased in the saturation regime we have:

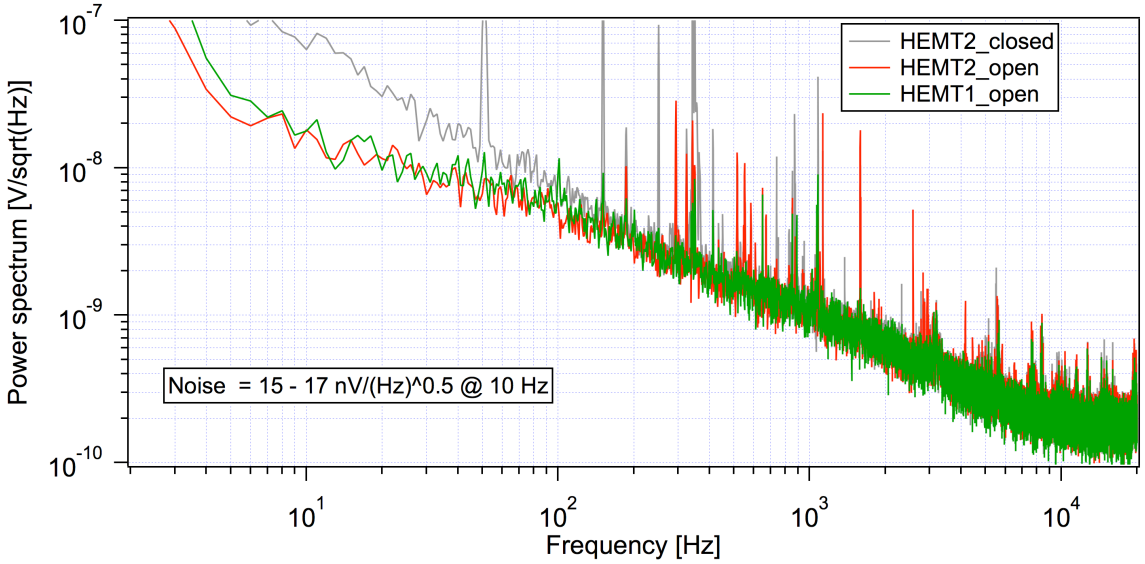
$\frac{-\Delta V_{ds}}{\Delta V_{gs}} \gg 1$ (typically 100 in our case).

We therefore obtain: $\Delta V_s - \Delta V_d \simeq 100 \cdot (\Delta V_g - \Delta V_s)$ and neglecting for the moment the second transistor we get:

$$\Delta V_s = \frac{\Delta V_g}{1 + \frac{1}{100}} \approx \Delta V_g$$

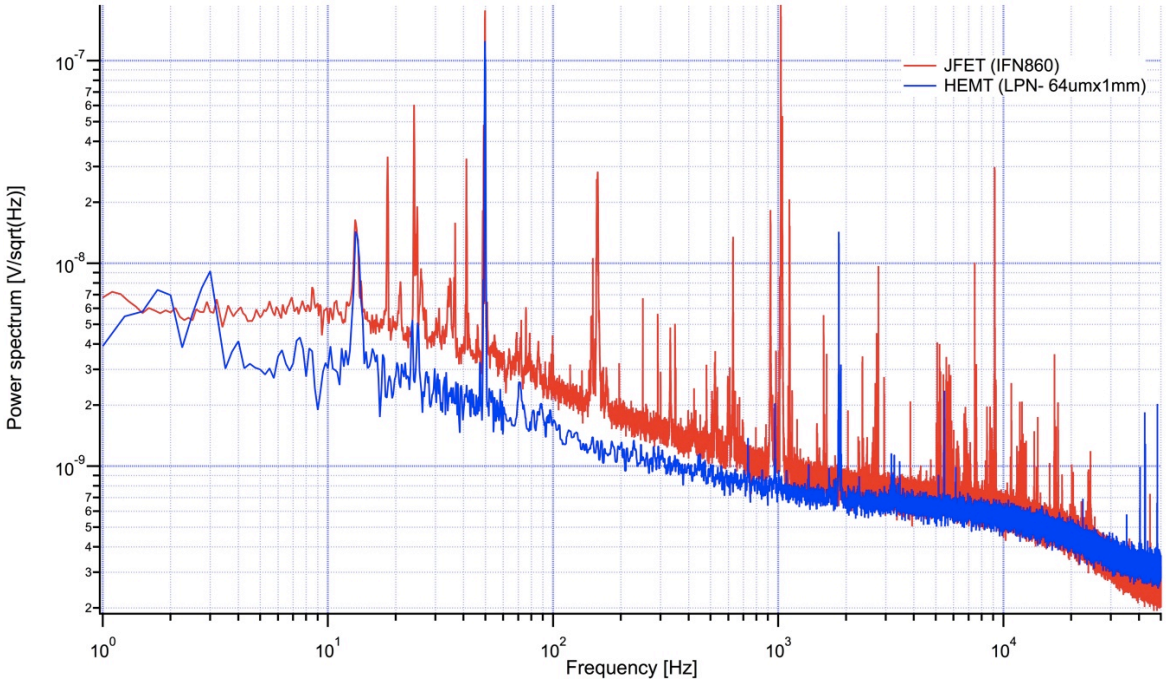
The amplitude of the source and gate signals is very close. ΔV_s is amplified by a factor of 50kW/50W using a OPA2227 chip. If the second HEMT is also biased in its saturation regime then: $\Delta V_d \approx \Delta V_s \approx \Delta V_g$. As a result the Miller effect of the input stage HEMT is very small.

The noise behavior of this setup is illustrated in the following figure. The two HEMTs have very similar characteristics and exhibit reduced noise amplitude below 100Hz in the 100pF mode.



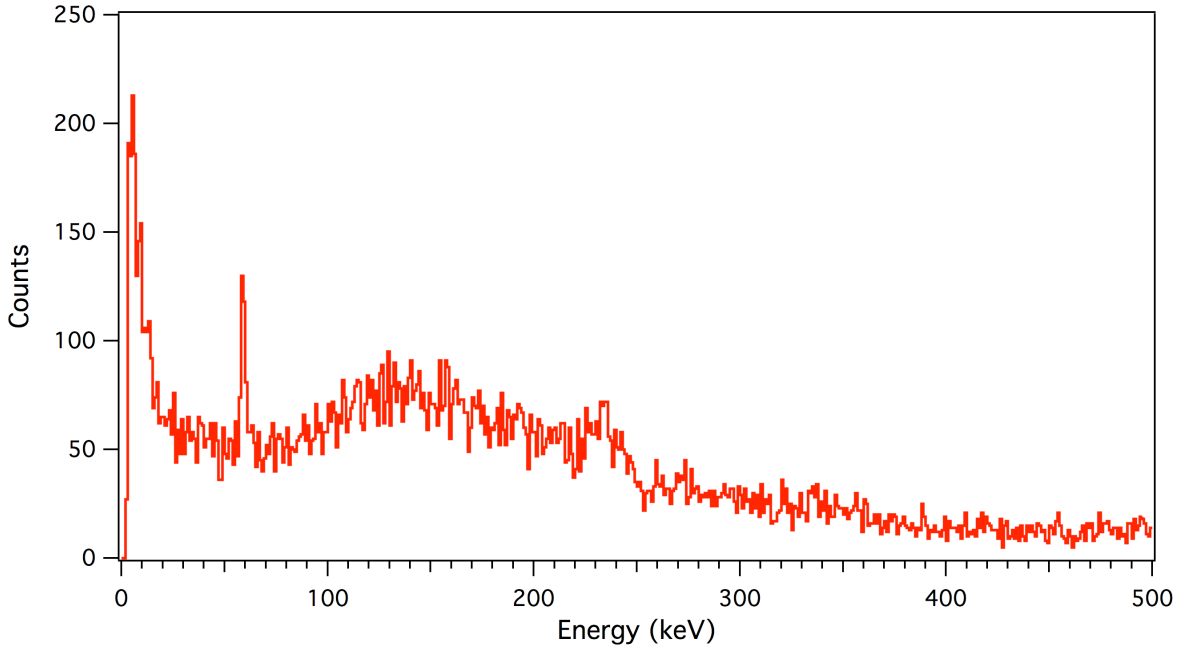
A comparison between the HEMTs used in the present work and typical low noise commercial JFETs (IFN860) is shown in the following figure. Both curves are measured with 100pF

capacitive load on the gate. The low frequency 1/f noise is related to the current noise of the transistors. The operating temperature of the IFN860 JFET was fixed at 150K.



2.3.1 Ge detector with HEMT front-end electronics

For the final test of the CESAR HEMTs we used a high purity 200g Ge detector equipped with a calibration ^{241}Am source giving a 60keV gamma line. The temperature of the detector was regulated to 20mK in order to simulate a cryogenic environment similar to that used in the EDELWEISS experiment. The energy spectrum measured with this setup is illustrated in the following figure.



The 60 keV line has a full width half maximum of 2 keV and is limited by the baseline resolution of the detector. The calculated HEMT charge amplifier performance should

nevertheless exhibit sub-keV resolution. Therefore, the observed resolution is most probably limited by the detector leakage current or cabling and connector parasitic noise. Further work is underway to limit these extra sources of noise and achieve HEMT performance limited operation.

2.3.2 Conclusion

In the frame of the CESAR program we have developped and tested cryogenic charge amplifier electronics based on HEMT front-end components. Operation of the HEMTs at 4.2K is very promishing with a measured amplifier performance improved by more that a factor of two compared to state of the art commercially available JFETs. Further work is needed to optimally couple our HEMT electronics to a cryogenic Ge or Si detector in order to propose an efficient alternative solution to very low temperature detection experiments.

2.4 Ge-JFets

2.4.1 Introduction

In the "CRYOGENIC ELECTRONICS FOR SPACE APPLICATIONS AND RESEARCH" FP7-project coordinated by CEA, the work package WP 2 is devoted to design, fabricate and supply various cryogenic Ge, SiGe and AsGa based transistors for front end readout electronics at T =4.2 K and to push their performance better than that of the current Si JFETs working at T > 100 K, in terms of low frequency noise, input capacitance and power consumption.

The CNRS-IEF partner is charged of the evaluation of a Ge based JFETs fabricated via an original approach based on gas immersion laser doping (GILD) of source, drain and gate areas. In contrast with the classical doping by ion implantation, the laser doping technique developed at IEF results in sharp interfaces similar to that obtained by epitaxial growth.

The first year (2011) was dedicated to preliminary experiments scheduled in the work program. The main issues to be adressed were :

- the cleaning of germanium substrates before epitaxial growth of the JFET channel,
- the UHV-CVD homoepitaxial growth of doped germanium,
- the superficial gas immersion laser doping (GILD),
- the formation of ohmic contacts on n and p types doped germanium.

All the problems associated to these technological steps were almost surrounded, particularly the GILD technique which was found to result in the expected doping levels and in very good ohmic contacts. It must be emphasized that getting ohmic contact on n-type Ge is rather challenging. On the contrary, the homoepitaxial growth of Ge proved to be more tricky than expected and consumed more time than initially scheduled. We had therefore to develop a two-temperatures procedure in order to reduce drastically the surface diffusion of adatoms at the very beginning of the growth. During the same period, a test Ge JFET was designed by using a classical simulation code. In this first design, the N^+ source, drain and P^+ grid areas of the JFET were to be achieved by localized superficial doping of a poorly doped Ge layer grown on a p^+ substrate.

The following of our work in 2012 consisted in the fabrication of complete test devices. An additional technological issue to be solved was the masking for GILD of source, drain and gate areas. The efficiency of the mask was appreciated through the threshold number of laser shots which it can withstand before being damaged.
Several runs were done to check the possibility of making devices with non-intentionally doped epitaxial layers. In this case, the thickness of the epilayers must be fixed at 1 micrometer. Tens of transistors were tested at room temperature, showing a sytematic residual current leakage. A more accurate observation of the epitaxial layer has evidenced a problem we believed to be solved : a noticeable density of pinholes through the n-i-d epitaxial layer. These pinholes are inversed pyramids delimited by (113) facets. A series of different cleaning procedures was tested : the chemical cleaning was repeated several times, the degasing temperature before growth were increased up to 800°C. We didn't succeed in decreasing significantly the density of pinholes, which remained in the range of 10^3 cm^{-2} in spite of the numerous tested cleaning and growth conditions

At this step (at the beginning of 2013), we considered that a drastic decreasing of pinhole density below a value compatible with macroscopic transistors should need a too long and uncertain study, and we proposed an alternative design for the Ge J-FET transistor, which was assumed to accommodate the observed density of pinholes.

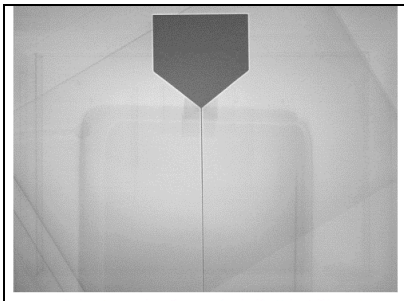
2.4.2 Development of SEG channel - Ge JFET.

In this alternative design the laser n-doping is made at the beginning of the process flow to form n^+-p^+ junctions on the p^+-doped substrate. A SiO_2 layer is then deposited. A window being opened through the silica layer, the n^+-doped layer is partially etched and a selective epitaxial growth is done in the window to form a non-intentionally-doped channel between two n^+-doped layers. As epitaxy is done only in between the back and front gates, there is no default due to pinholes through the epitaxial layer.

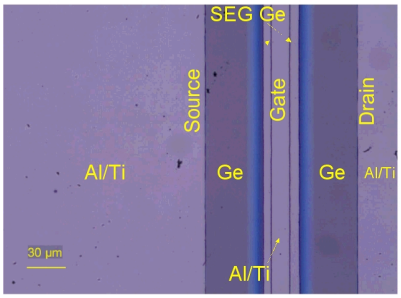
From our first model, it is possible to obtain a modulation of the JFET current with a 1 micrometer thick non-intentionally-doped channel. For thinner channels, a low n-dopant concentration (5 x10^{16} cm^{-3} @ 300nm) is needed in order to limit the electrical field below its breakdown value. As it is not possible to dope by GILD a layer as thick as 1 micrometer, we choose to use the GILD technique for introducing the donors both in the S&D and in the gate areas. Starting from P^+ Ge substrates and PCl_3 as dopant gas, 3 to 10 laser shots were found to result in 350 nm N^+ doped layers. Rectifying behaviours of the resulting p-n contacts proved than the initial doping concentration of boron dopants in the substrate was compensated. The gate region must be then etched in order to leave 1.5 $10^{12}/cm^2$ donnors in the channel, which corresponds to a final thickness of 100 nm. The etching rate of Ge in hydrogen peroxide was found to not depend on the number of laser shots (i.e. the doping level).

The step of selective epitaxial being validated (Fig. below), complete test devices were metallized and tested at room temperature. I(V) characteristics evidenced currents in excess in reverse bias. That occurs before reaching the saturation of I_{DS} at V_{DG}=0, and before reaching I_{DS} pinch off for V_{DG}. It is therefore not possible to check the transistors at room temperature. This behaviour is probably due to tunneling effect through the

(too thin) depleted layer between n^+ and p^+ domains. This issue may be avoided by reducing the ionization of dopant impurities. So, tests at low temperature must be scheduled in a next future.

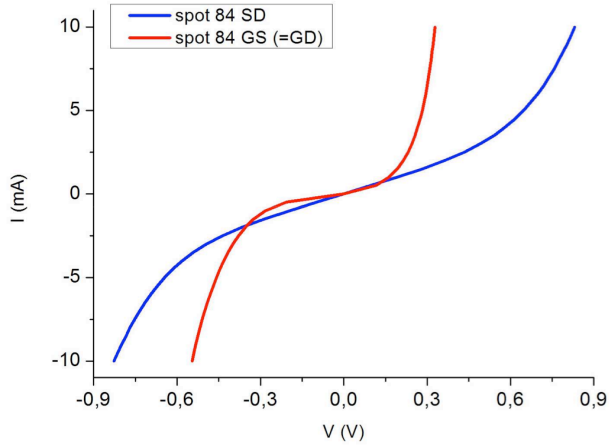


(a)



(b)

Views of JFET transistors after selective epitaxial growth of the Ge channel (a) and after metal deposition (b)



I_{DS} (V_{DS}) and I_{GS}(V_{GS}) measurements at room temperature. As expected, I_{DS} is linear at V_{GS} =0, but leakage currents are found at too low voltages and the saturation is not reached. The voltage strength of the G to D (resp S) contact is very low in reverse bias. This may result of tunneling through the depleted layer in between p+ and n+ domains.

2.4.3 Study of GILD-based ohmic contacts.

In parallel with the development of JFETs, the study of ohmic contacts on Ge has been continued. The corresponding results are reported in references [1] and [2]. We achieved ohmic contacts down to low temperature (10K) on standard n-doped Ge by creating between the metallic contact and the Ge substrate a strongly doped thin Ge layer. Thanks to the laser doping technique, we could easily attain extremely high doping levels, above the solubility limit, and thus reduce the metal/doped Ge interface resistance at room temperature to values as low as 5 $x10^{-6}$ Ω cm^2. We independently tested the influence of the doped layer thickness and dopant concentration on the metal/doped Ge interface resistance, showing that the ohmic contact is robust when changing the metal, the doped thickness and improves when increasing the doping level. We also characterized the n^{++}Ge / n Ge contact, showing that its interface resistance, independent on doping thickness and concentration, is for high doping the dominant contribution in the contact.

A specific approach was used to determine separately the respective interface resistivities between metal and n^{++} doped layer (R_CM/n^{++}) and between n doped Ge and n^{++} doped Ge (R_Cn/n^{++}). This approach is based on the comparison of resistance measurements before and after etching of the superficial doped layer. In the unetched bilayers most of the current is transmitted through the thin doped layer and the corresponding R(L) dependence fits mostly the thin limit approximation corresponding to a linear R(L). We have modelled the etched samples in the intermediate thickness regime and found, by fitting the numerical simulations, an analytical expression that enables us to determine R_Cn/n^{++} .

3 Complex Circuits (WP3)

3.1 CMOS

In the first period, a standard CMOS technology (TSMC 0.18um) was selected after tests on single transistors. Two design iterations for DAC and amplifier chip have been performed, one design iteration for ADC.

During the last period of CESAR, functionality measurements have been performed at cryogenic temperatures at basic building blocks designed and manufactured during previous periods. These building blocks include single transistors as well as VGA, input buffer and DAC. Since the measured behavior of the building blocks does not meet the simulated performance at 4K, the performance lies outside the specifications.

Detailed measurements have been performed on the building blocks input buffer, VGA and DAC in order to understand the erratic behavior. The outcome of the measurement analysis is used during the design of the final CMOS ASIC T10.

The CESAR system has an integrated multiplexer, multiplexing 16 pixels in 1 output channel. Furthermore, since the power consumption of the ADC is sufficiently low if operated at the appropriate frequency, the CESAR system can be designed including a limited amount of ADCs for each 16 channels. Therefore, there‘s no longer a need to design a dedicated multiplexer circuit for the CESAR system.

A final version of the 4K and 20K ASIC have been designed. The 4K ASIC includes the full system of input buffer, DAC, and VGA. Furthermore, a separate DAC and input buffer have been implemented on the ASIC for testing purposes. This allows a separate characterization of these building blocks.

The 20K ASIC includes per channel an input buffer, a low-pass filter and an output buffer. 18 Channels have been implemented on this ASIC, so the final instrument will require only 1 20K ASIC per detector array.

Special attention has been given to maximize simplification of the amplifier architecture, transistor matching, transistor biasing outside problematic freeze-out regions, and configurability to circumvent possible performance degradation at cryogenic temperatures.

Simulations have been performed using 300K and 4K models, and have shown a simulated performance according to specifications.

Both ASICs, 4K and 20K, have been taped out in TSMC 0.18um technology; assembled in JLCC test packages.

Testing of final ultralow power cryogenic ADC and DAC

Upon arrival of the assembled test devices, IMEC has performed a functionality check and characterization of the devices at room temperature. All test structures (input buffer, VGA, DAC)

as well as the 4K system and 20K system ASIC have shown behavior which corresponds with the simulation results.

Afterwards the test devices were shipped to Konkoly, including a description of the devices and recommendations for testing.

Konkoly has performed cryogenic measurements on the 20K and 4K ASICs. Satisfying results were obtained for the VGA, input buffers and 20K system. Further reporting needs to be made. Concerning the DAC, the first measurements with default clocking diagram did not give a linear output. Further measurements were planned with modified timing parameters for better understanding. The final testing at Konkoly using the modified timing diagram, resulted in successful characterization at 4K.

3.2 SiGe

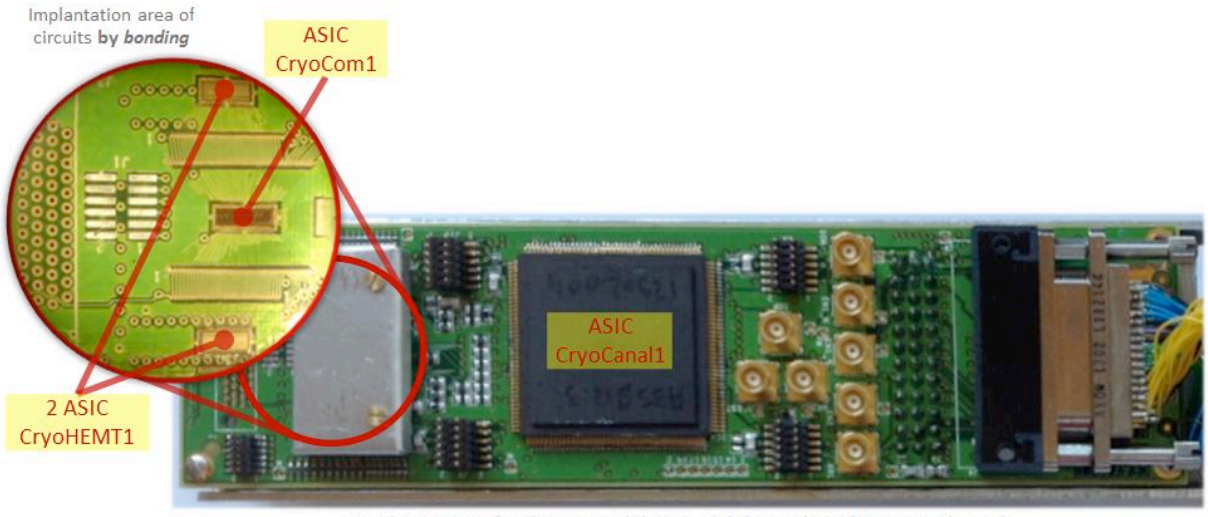
The last periodic report ended by the delivery (December 2012) of two new ASICs, *CryoCom1* and *CryoCanal1*, designed by CEA-IRFU-SEDI and produced by AMS foundry in its 0.35 µM SiGe BiCMOS technology. These two ASICs were the main elements of the new version of the electronics, which improves the performances and features of the first one.

Since this date our activity was focused on the development of the new test bench, designed to validate these new circuits and evaluate their performances, and on the tests themselves.

The new test bench contains four elements : an electronic board designed to implement the new ASICs, a mechanical system to allow the cooling of the electronics for its test, different boxes and board for powering, signal outputting and control, and a software to control the board from a computer.

3.2.1 Test electronic boards.

Two boards have been developed. The first one, *CryoTest1*, is designed to receive and implement the new ASICS. One of these ASICs (*CryoCanal1*) has been packaged and it is soldered in its package on the board, while the three others (two *Cryo17HEMT1* and one *CryoCom1*) are bonded directly on the board, without package, as they will be in the final system for very large scale integration reasons.



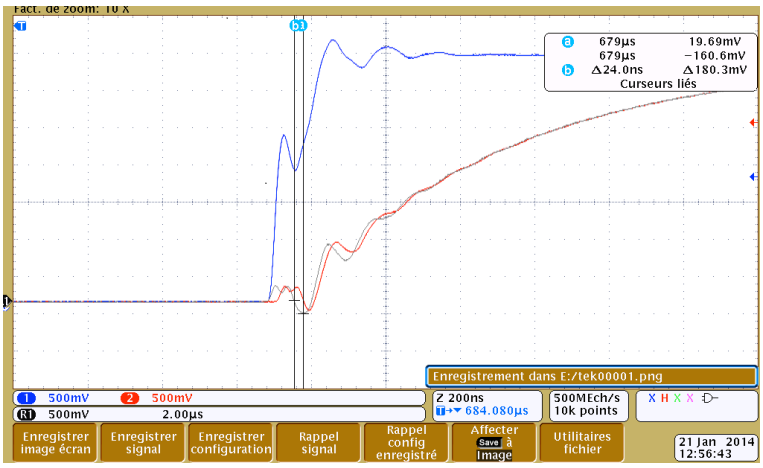
Board CryoTest1 : for the ASICs validation, and the reading of 34 to 128 channels

This board is designed to test and validate the ASICs, but also to be used in a second time as a first acquisition tool. Indeed it can be used to read until 32 detector channels, but coupled to a partially equipped flexible PCB it will be able to acquire until 128 channels.

3.2.2 Tests.

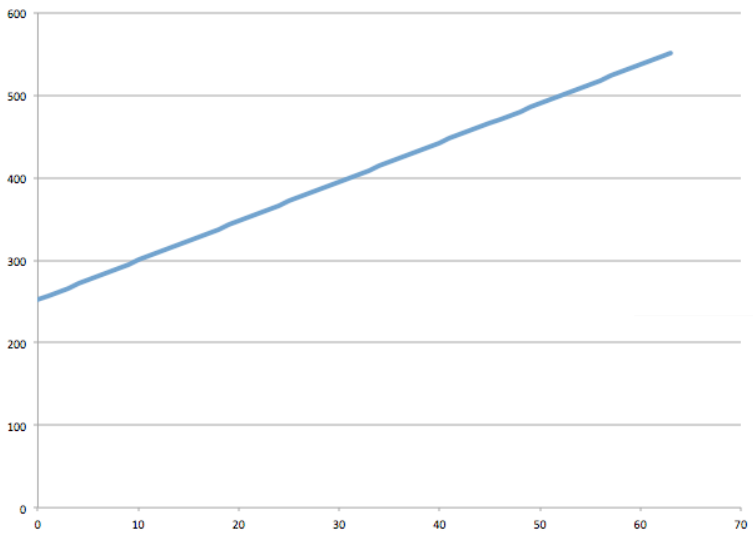
The first step of the test was to validate the writing and reading in all the registers of both ASICs (*CryoCom1* and *CryoCanal1*), and particularly to test the functioning of the new communication protocol that includes a decoding of circuit address. This step has been entirely validated.

The second step was to control that the registers configure correctly the sequencer, and that this sequencer works properly. This sequencer generates the internal clocks of the ASIC, which drive the scanning of the input channels for time multiplexing. The time separation between clocks, which can modified by slow control, has also been controlled. All works properly.



Control of the time separation between two clocks (blue and red), for two values of delay fixed by slow control (compare red and grey).

The third step was to verify that the internal registers control effectively the other functions of the ASICs. For example, we controlled that the configuration of the electronics (working mode, scanned channels, etc.) is modified as expected when the registers are written, and the same for the value of the internal voltage references, generated by internal digital analog converters. This step is on the point to be completely tested (only the baseline equalizer and the test signal output driver remain to test).

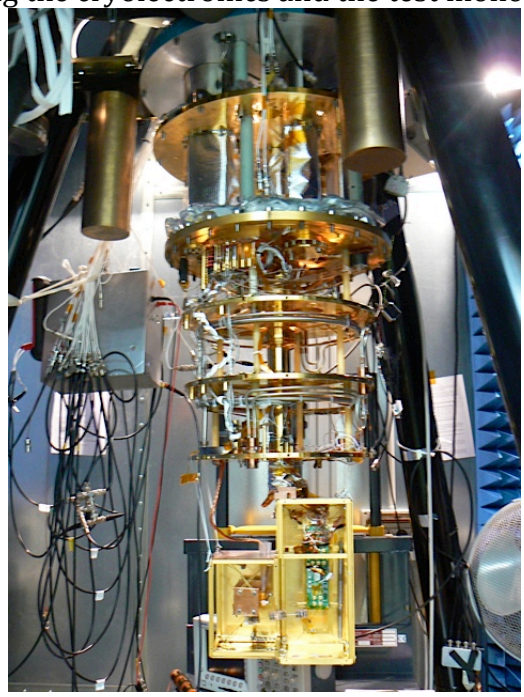


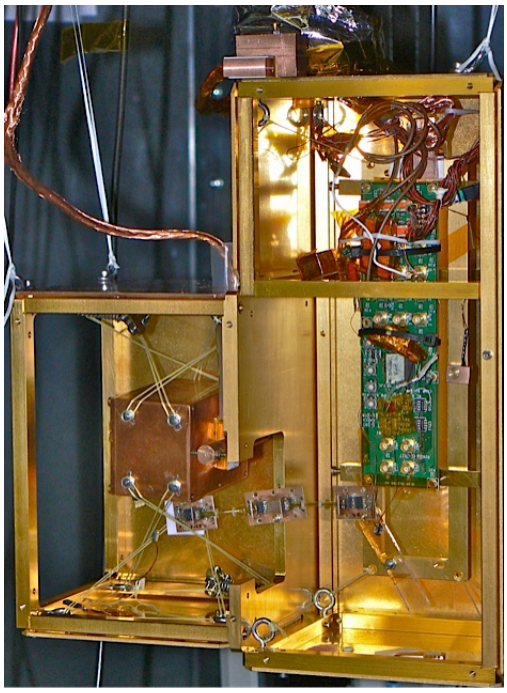
Output voltage of one of the internal 5-bits digital analog converters (ordinates), according to input digital value (abscises).

The next step, which is in progress, is the test of the analog parts of the ASICs, in their different modes.

4 X-Ray Microcalorimeters (WP4)

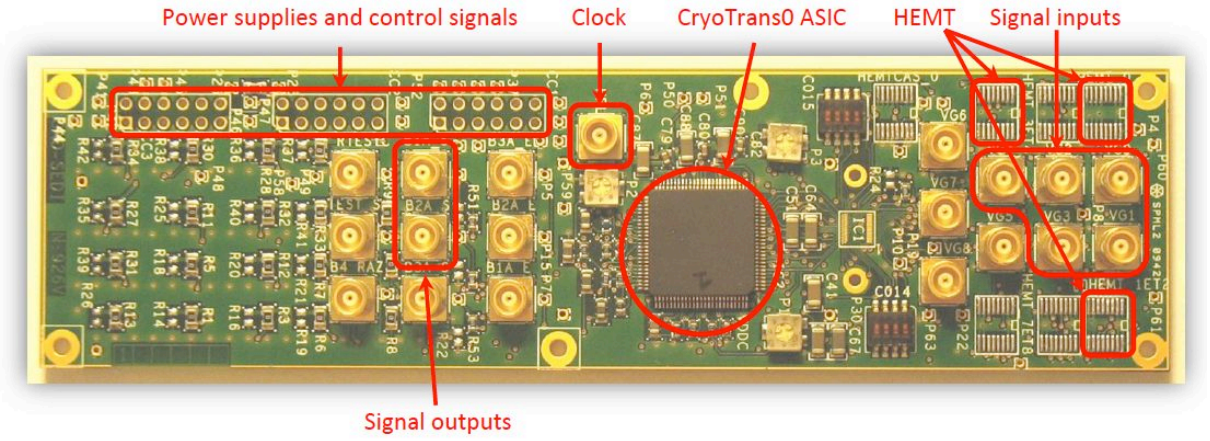
The upgrade of the Saclay facility has been completed; the suspended Faraday cage is housing the cryolectronics and the test monopixel microcalorimeter.





The construction of the shielded room at UNIPA (Palermo) has been completed, the ADR cryostat has been installed and the system wiring has been optimized to reduce noise; an Isolation transformer has been installed, line filters have been installed and the grounding circuit has been carefully designed. This facility is now fully operational.

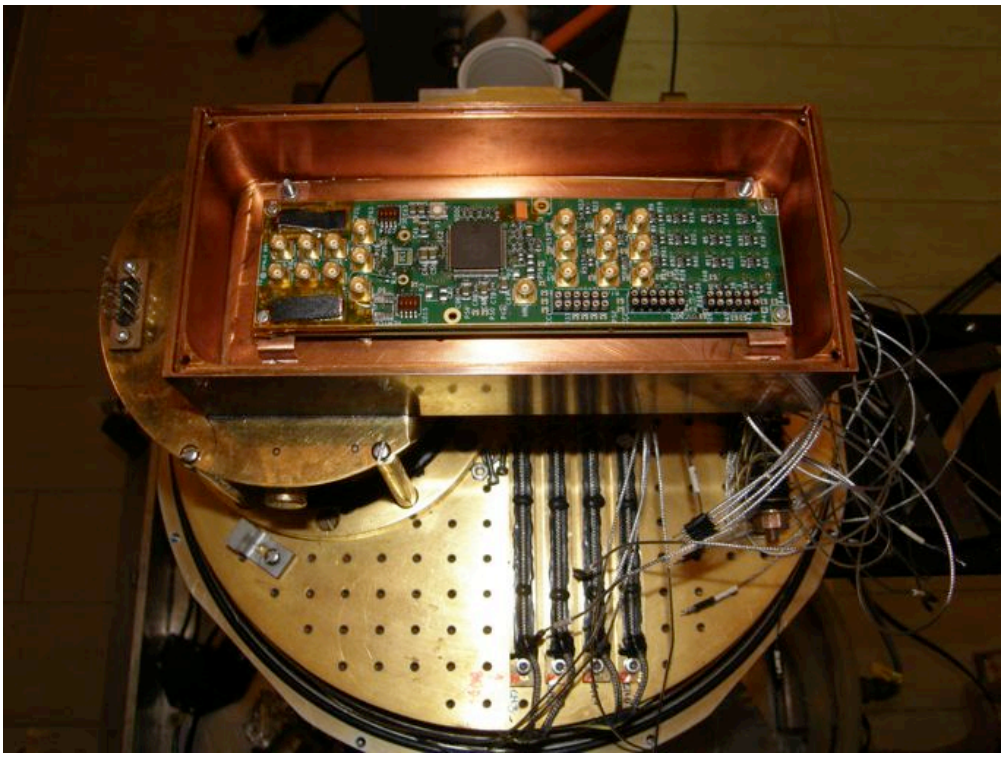
The cold electronics, in the Cryotrans0 version, has been tested and the measurements of its performances in terms of noise versus frequency are satisfactory. The power supply, the controller interface and the control software have been developed as part of the test environment.



The Cryotrans0 cold electronics, its test set-up and operation manual have been delivered to UNIPA.

Ugo Lo Cicero from UNIPA has been trained in Saclay on the Cryotrans0 cold electronics and its test set-up at the beginning of May.

The Cryotrans0 board has been integrated and is being wired inside the UNIPA cryostat.



A test array of four NTD Ge microcalorimeters have been tested with front end HEMT's.

HEMT's exhibit a much lower noise than the JFET's they replace.
Testing of the full chain should begin in June 2014.

5 Far-Infrared and Magnetometry (WP5)

5.1 Far Infrared

5.1.1 Introduction

The goal of this work package is the realization of a complete electronic chain equivalent to the PACS (Photodetector Array Camera and Spectrometer) bolometer array electronics aboard the Herschel space observatory, but where all the signal processing is made at cryogenic temperature.
During the Herschel-PACS project new detector arrays were developed, by the Saclay group, to achieve large focal planes with thousands of pixels detecting in the sub-millimetre domain. It was at the time a major step: the largest bolometer arrays for ground or space applications were only made with few tenths to few hundreds detectors.
For sensitivity reasons these detectors are located at the heart of a cryostat at very low temperature (around three tenths of degree Kelvin above the absolute zero) and surrounded by different temperature stages : 2 K (superfluid Helium), 4K (normal Helium), 20-40K(pulse tubes) and 150K (shields).
The number of electronics channels dedicated to read these detectors arrays, was an issue for two reasons, both linked to the very limited power budget available at such temperature in space.
The first reason is the number of wires going from the very cold bolometer detectors in the focal plane, to the warm temperature electronics outside the cryostat. A minimum of three wires per pixel is required to bias each detector and to read it. Even if we can distribute the biases adapted for each array collectively, the number of outputs (256 per array) is sufficient to load the cold stage with more power than can be extracted by the cryo-coolers developed for space applications.
The second reason is the electric power dissipated by the analogue electronics itself: if each detector is linked to its own circuit. A rule of thumbs shows that the total required electric power (even at warm temperature) is not compatible with the budget available in a space observatory.

Multiplexing is mandatory.

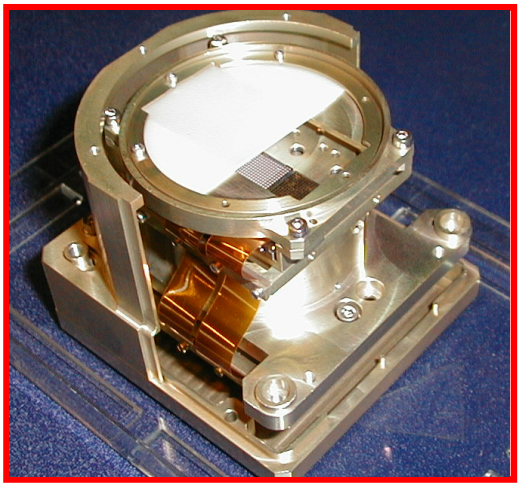
On PACS, the multiplexing (x 16) and detector impedance adaptation was done at very low temperature (300mK and 2K), as close as possible of the detector sensors to avoid signal degradation on the high impedance side of the circuit. It was a first step in cryogenic electronics, allowed by the high signal level foreseen on the targeted astronomic sources. Nevertheless, we experienced perturbations induced all along the 10 m wires. The fast switching (3kHz) of the solar panels was one of the identified sources, the other being generated by the communication between the satellite and ground stations.
In the next space observatories this will not be sufficient. For example, in the sub mm and mm domain, the signal in the B-modes of the Cosmologic Microwave Background (CMB), is few orders of magnitude below the thermal fluctuations measured by Planck or WMAP. This faint signal must be preserved from any contamination. Our analysis was that, in the next Space observatories, all the signal processing must be done at cold level, in order to communicate only through robust digital links.

We proposed to IMEC (Belgium) to develop a complete analogue electronic chain, including ADC, working at cryogenic temperatures (4K-20K) to complete the detector multiplexing and impedance adaptation already implemented on PACS. We asked the Konkoly Observatory to participate to this demonstration, taking advantage of the excellent work made during the Herschel radiation tolerance analysis on ground tests and during flight operations. As spare detector arrays from the PACS project were still available, we decided to include this action in a larger program dedicated to the development of cryogenic electronics from single elements (HEMTs, JFETs) to complex circuits (SiGe): CESAR.

Moreover, as the Space Development Policy has deeply evolved in fifteen years: the selection of any technological solution for a future project must have a Technological Readiness Level (TRL) equal to 5! (Validated in the proper environment). Before any instrument solution proposal, we must demonstrate a high maturity level. The purpose of the CESAR project is really a TRL rising procedure even leading to produce prototypes and in some cases demonstrators.

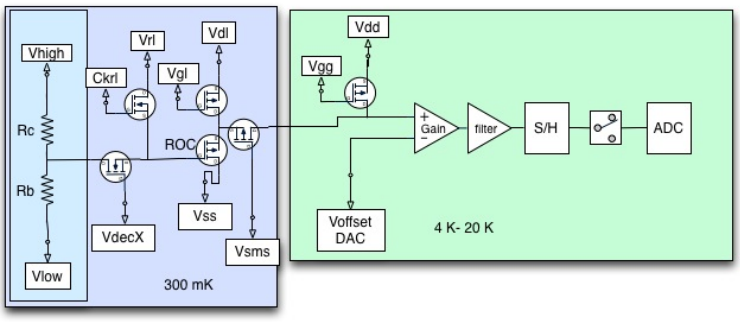
5.1.2 Development of the Saclay facility

The PACS bolometer focal plane assembly is a compact box (~10 cm)^3 containing the detector arrays hybridized to the cold multiplexing circuit and linked through internal ribbon cables to the 2 K readout circuit.



The PACS focal plane assembly with one detector array visible behind the filter layer and ribbon cables between 300 mK and 2K stages. The later stage contains the second impedance adaptation circuit (buffer).

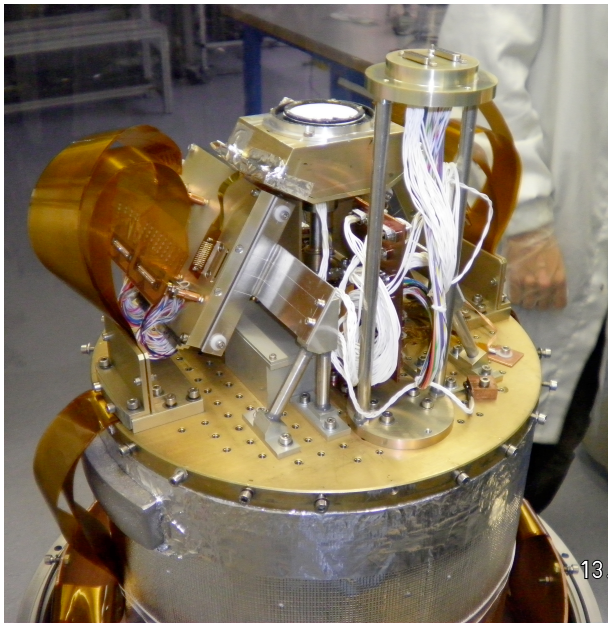
For the CESAR WP5 project, this solution is no longer suitable: the detectors and MUX circuits are mounted independently of the Board containing the entire signal processing at cold stage. This board must be located close to the detector (<10 cm) at a temperature not exceeding 20 K with a power budget of ~10 mW, and to be realistic with respect to the volume available around the focal plane in a Space Observatory, a 10cm x 10cm x 1 cm board size was agreed between partners.
The functional requirements on this board are given in the scheme below:



Requirements on the signal processing board (green). The blue part is the existing bolometer array with its MUX and impedance adaptation (only one channel shown).

The first required function for the board is the bias of the 300 mK MOS transistor (left) for impedance adaptation (ROC) by two voltage commands Vdd and Vgg. The second function is an offset compensation by a local DAC (Digital/Analogue Converter), local is required because the noise level of this compensation voltage must be as low as possible (much lower than the signal noise). After, a gain and filtering stage adapts the signal level to the ADC (Analogue/Digital Converter). In between a Sample and Hold (S/H) guarantee the sampling simultaneity of all the detectors having the same address (colon wise).

We built a new test cryostat to host the CESAR developments with functions very close of the PACS one. The sensitivity being the pertinent parameter of this development, response and noise must be computed from measurements at different fluxes and compared to the initial PACS solution.



the CESAR test setup *as built*.

On the 4 K plateau of a "wet" cryostat, the detector array enclosure is mounted on the ^{3}He cryocooler. A filter (the white patch in the figure) protects the detectors and selects the needed optical bandwidth. In front, not shown in the picture, the optical bench comprises two blackbodies with different solid angles separated by a chopper to modulate the flux in the "small signal" regime.

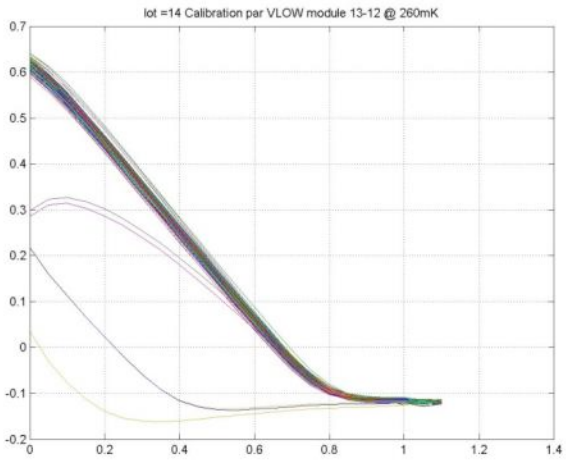
A thin ribbon cable, on the left side of the detector enclosure is plugged in a square shaped yellow box. This box is the location of the IMEC Board. The temperature of this box can be regulated to any level from 4 K to 20 K through a resistor patch. The large harnesses, on the left, collect the digital outputs from the board and provide, the two cold stages, with biases and clocks.

A fair comparison between the previous electronic architecture and the CESAR one supposes that all the components of the PACS scheme must be integrated in the CESAR setup. The PACS 2K circuit (that assumes the second impedance adaptation :BU- for Buffer Unit) have to be introduced in the new test configuration. An electronic board (PCB) with same mechanical and thermal interfaces was developed: the NaBU. On this board, the CMOS chip is simply hybridized by In bumps.

5.1.3 The test procedure & results

The detector array selected for the CESAR project (SMD 100_13-12/14) manufactured by Leti in Grenoble is tested applying the PACS procedures in the "PACS like configuration".

STEP #1: *electrical calibration.* In this step we compute the transfer function of all the electronic channel by biasing the bolometer with Vhigh = Vlow from zero to 1 volt. Under these conditions the detector output is equal to the input (usual output conditions), and recording the final output voltages after impedance adaptation, gain and filtering stages.



electric transfer function of the different pixels in the array. The X axis is the input voltage, the Y axis is the output voltage.

STEP #2: Flux response, noise and sensitivity.

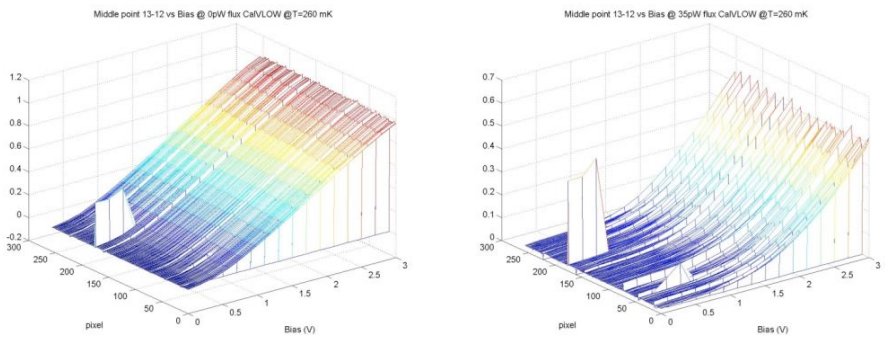
The detector array is exposed to increasing sub-mm fluxes [0 5 15 25 35 pW]. For each flux, we explore all the biases between 0 and 3.4 V by 0.2 V steps. During this process, after few minutes of stabilization once the bias is set, we record the signal output for 60 seconds. From the signal *level* we obtain the detector responses after comparison with the other fluxes. From the *time sequence*, we extract a noise spectrum at the given flux.

Cryogenic detectors are very dependent of the temperature. The final temperature of use depends strongly on the detector load. We are by consequence obliged to re-do the complete test set at three temperatures: the low and high values (260 & 300 mK) and the most probable temperature of use (280 mK). Here for the CESAR demonstration we have performed measurements only at 260 mK (the most critical temperature).

5.1.4 RESPONSE:

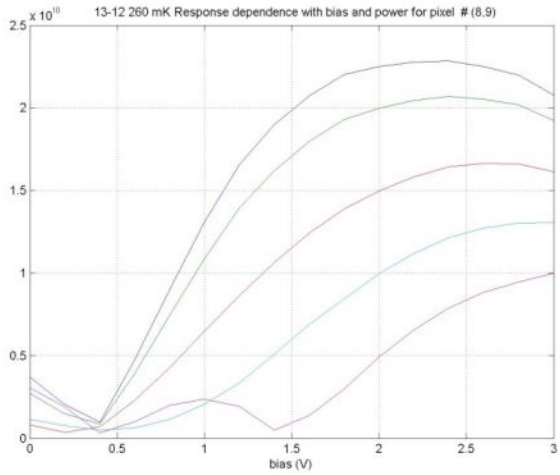
In a bolometer bridge, the resistance of the sensitive part of the detector varies with the absorbed flux. In our peculiar system, the resistances (bolometer and charge resistor) vary also with electric field (i.e. voltage across the resistive sensor).

Nevertheless, the signal is given by the voltage variations of the middle point of the resistor bridge. The first operation is to compute, for all the 256 pixels, the middle point voltage at each bias voltage, with respect to the low-end voltage of the bolometer resistor bridge. At this stage, the *electric calibration* (step #1) is needed.



Middle point voltage output for all the pixels at different biases for two extreme optical situations : 0 and 35 pW of incident flux.

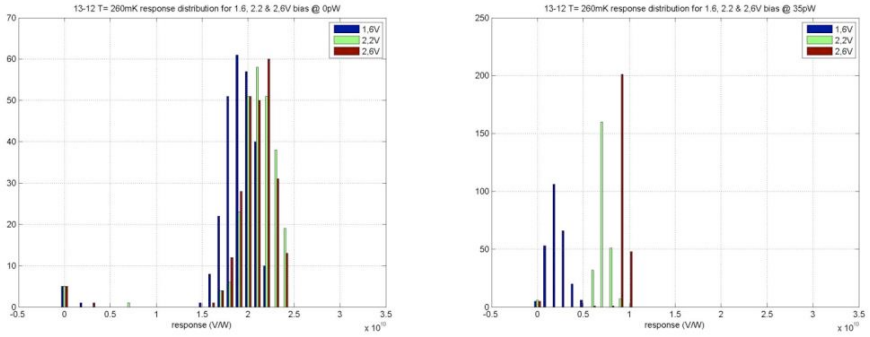
The figure above shows the voltage of the middle point of the detector resistor bridge for each pixel of the array, at 0 and 35 pW of sub-mm flux for different biases. From these measurements, for each pixel, we can deduce the detector response as shown in the figure below.



Detector response (V/W) dependence with bias for different fluxes: from figure top to bottom 0, 5, 15, 25 and 35 pW.

As usual for a bolometer, the response decreases with absorbed power, and the optimum bias shifts toward high bias with increasing power: 2,2V at 0 pW and more than 3V for 35 pW.

At this level, statistics can be made for the pixels population. Hereafter the response histograms at different biases (1.6, 2.2,and 2.6 V) , in two extreme conditions 0 and 35pW/pixel.

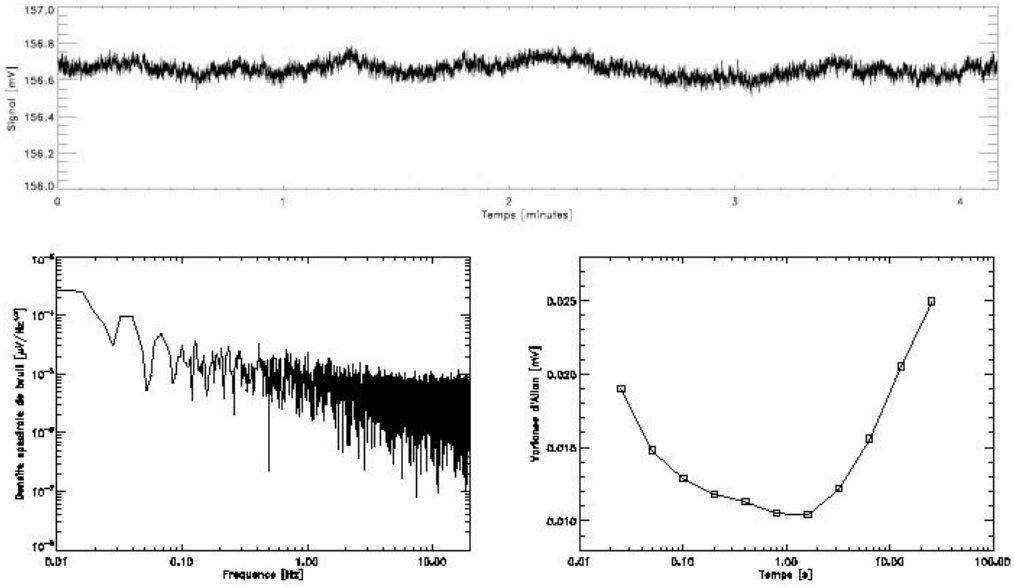


Detector response (V/W) histograms at different biases under extreme fluxes.

For the same array, the response distribution, at low flux has a low dependence with bias. This is not the case at high flux where the higher bias is strongly favoured.

5.1.5 NOISE & SENSITIVITY:

From the 60 seconds output recording, a well-calibrated Fast Fourier Transform, produces the noise spectrum for each pixel. This spectrum shows in general two regimes: the white noise, “flat” as expected and a low frequency behaviour commonly called “1/f” noise. The slope and the “knee” position between these two regimes are rather important. Here a typical time sequence and its spectrum.



The time sequence and the correspondent frequency spectrum with “knee”. Lower right the Allan variance gives at its minimum the optimal coherence time of the signal

Once the response computed and the noise density evaluated for each pixel, all the ingredients of the sensitivity are ready for use. The Noise Equivalent Power (NEP) is simply the ratio of the noise density at a given frequency, by the detector response.

Of course, the sensitivity is obtained for a given detector **temperature**, **bias**, **flux** and **frequency**.

The next figure is the sensitivity distribution of the array at 260 mK with bias= 2.6V for the noise density evaluated at three positions: 1, 3, 5 Hz under two extreme fluxes [0 & 35pW/pixel].

As foreseen the sensitivity is lower (better) when the detectors are unloaded by flux, and better un the white noise regime that in the low frequency part of the spectrum.

5.1.6 Conclusion

Today, the test setup is built and perfectly operational in Saclay. The operability was tested in a PACS like configuration. The PACS like configuration preserve all the cryogenic electronic chain but in a very different mechanical architecture: the detectors and readouts circuits at 300 mK are no longer in a *all in one* focal plane assembly, but split in two boxes. In our CESAR configuration, the 2K circuit is located exactly in the same configuration that the CESAR foreseen final cryogenic electronic board.

The performances tests made on the detector array devoted to the CESAR project have been performed with the same procedure than the PACS ones.

The measurements give results equivalents to the previous bolometer used in the PACS Project. The next step this summer is to replace the 2 kelvin board (NaBU) by the IMEC board, and restart the same test procedure.

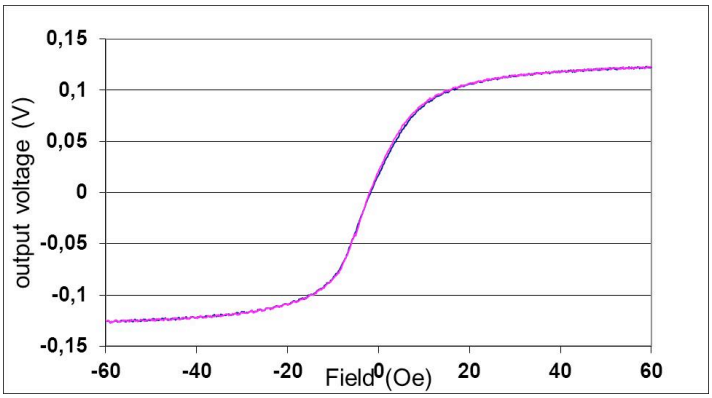
5.2 magnetometry

5.2.1 Introduction

This deliverable describes the work performed for developing a highly sensitive magnetometer for space applications based on spin electronics sensors with cold electronics.

5.2.2 Design of magnetometers

During the project several designs have been proposed and tested. The aim was to obtain a compact design able to fit inside the coils of imperial college and rather insensitive to temperature gradients.
The actual size of each magnetometer is 2.5x3x10mm with a typical response given in figure below.



Typical response of magnetic sensors bridges

The sensitivity of the present generation is 80V/T for 1V on the bridge.

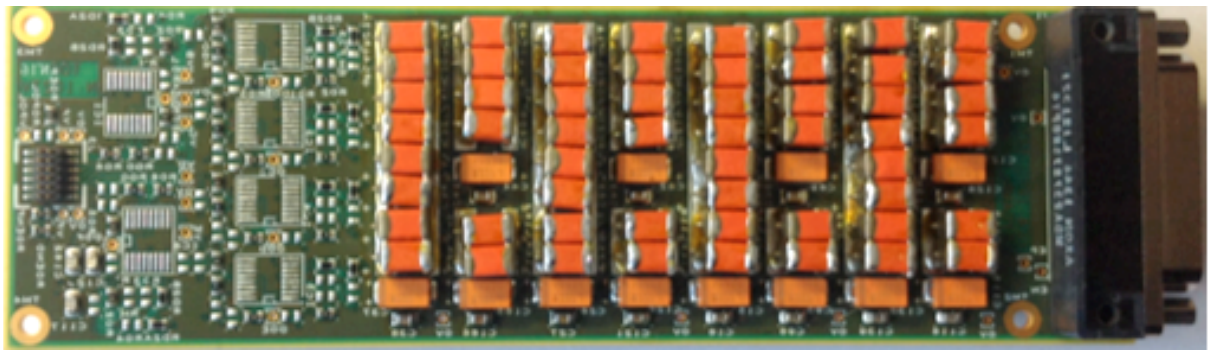
5.2.3 Temperature and Long term drift

During the first period, it appeared that temperature dependence of sensors is crucial for reliable measurements. First bridges tested in Imperial college showed a big temperature dependence.
A lot of work has been performed and it is still in continuation to improve that point.
The main reason is that the overall sensitivity of the sensors is typically now 8%/mT and the temperature coefficient of the main resistance is 0.3%/°C. This gives a temperature sensitivity of 37µT/°C so if we target 0.1nT/°C we must have a matching of

the GMR bridge in the range of 2 10^{-6} which is extremely difficult without a very precise laser trimming done in absence of external field.
Present technology without laser trimming allows us to obtain 10^{-4} in terms of matching by a sorting of GMR devices.
An alternative was to constantly monitor the mean resistance of the bridge in addition with the signal measurement and perform a data correction of the measured value. This has allowed us to gain a factor of about 30 on the thermal drift impact on data.
At present, we are focusing on a double optimization : laser trimming and bridge resistance variation correction.
The variation in temperature of the sensitivity is corrected by means of a closed loop scheme. The sensor bridge works always at the same point and the field is determined by the injected current of the feedback loop.

5.2.4 Cold Amplifier noise performances and gain

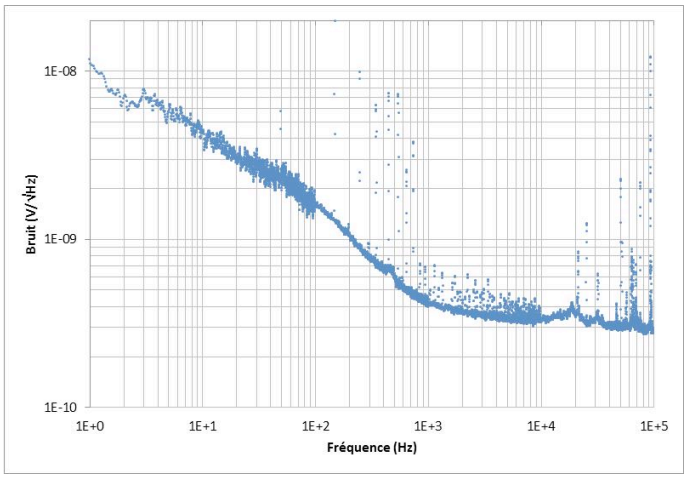
The electronic board that was designed by CEA-SEDI, called *CryoAmpliHEMT1*, consists in a 6-channels ultra-low noise amplifier (for the differential readout of 3-axes magnetometer), using HEMT transistors.



The *CryoAmpliHEMT1* board.

This board has been tested at 4.2 K. It has a gain of ~50, and excellent noise performances, which fully fulfils requirements :

1.6 nV/sqrt(Hz) at 100 Hz
0.42 nV/sqrt(Hz) at 1 kHz
0.32 nV/sqrt(Hz) at 10 kHz

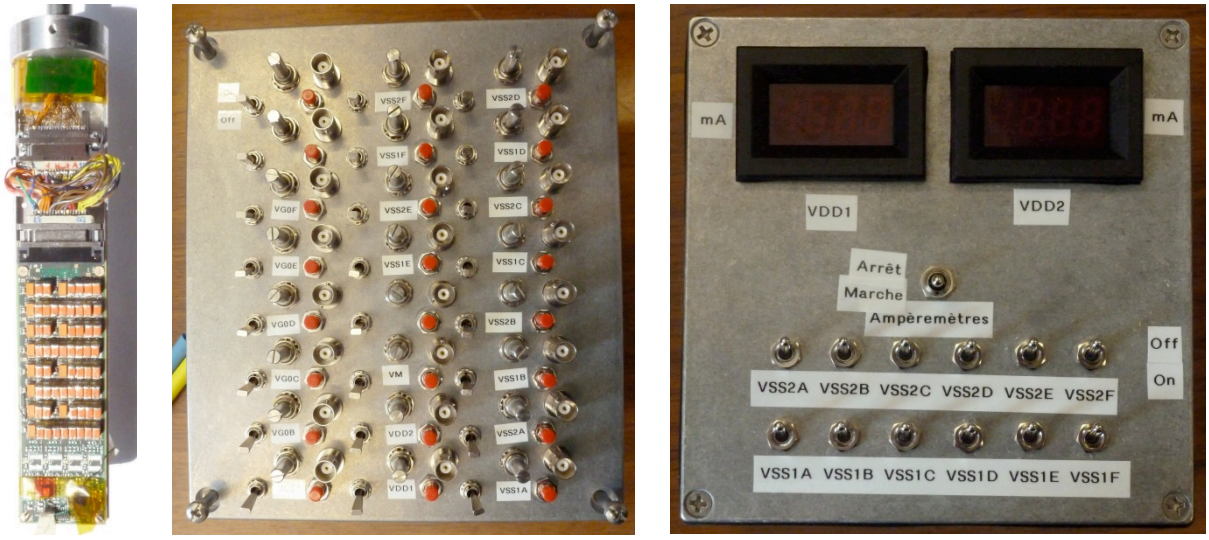


Noise spectrum at 4.2 K

The board was delivered along with several other related equipment :

- a low noise power supplies box, generating all the needed power supplies from a battery,
- an adjusting board, integrating two voltmeters and a set of switches, to ease the adjustment of the supply voltages.

This equipment is ready to use and available from end of March 2014.



The three elements delivered for magnetometry : the board, the power supply box, and the adjusting box.

5.2.5 Conclusion

If the objectives of the *Magnetometry Application* remain the same: produce very sensitive 3D magnetometers for planetology applications, the way to fulfil the specifications has strongly evolved during the CESAR Project duration. This was made possible thanks to a cooperative project scheme gathering people from different scientific and technical development fields, who have not very frequently occasions to talk together. The HEMTs transistors associated with SiGe circuits was not initially foreseen, mainly because the need for very low operational temperatures. It became an option when we understood that the gain procured by this solution overcomes the very low temperature cryogenic drawback. In return, working at very low temperature, allowed the use of superconducting structures that enhance the quality of the initial sensors.

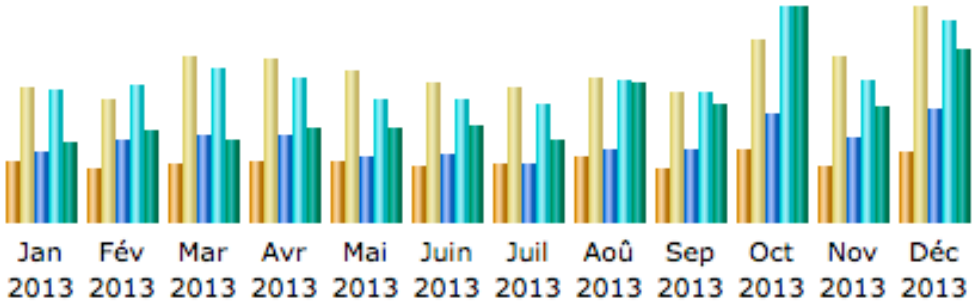
The electronic boards have been developed, manufactured, and delivered to scientists during the CESAR duration. The scientific benefit evaluation will take months after the end of the CESAR Project. Today, this solution is not yet accepted by Space Agencies as standard way to measure the magnetic field direction and intensity. But a demonstrator was built in the course of the CESAR program, allowing to present this solution with a Technological readiness Level quite high (TRL≈5) for future missions.

6 Exploitation and Dissemination (WP6)

6.1 Website

The CESAR website (www.cesar-space.eu) has been created at the beginning of the project, in order to present the partners, the work packages and goals of CESAR. The modifications throughout the duration of CESAR included light design changes, links to CESAR publications and links to CESAR public documents.

There are two tools that enable the monitoring of traffic statistics and requests on CESAR public website. The first one is developed by CEA (figure 1). The second one is the "Google webmaster tool".



Mois	Visiteurs différents	Visites	Pages	Hits	Bande passante
Jan 2013	130	288	892	1 659	41.15 Mo
Fév 2013	115	263	1 045	1 713	46.53 Mo
Mar 2013	126	353	1 086	1 916	41.22 Mo
Avr 2013	128	348	1 106	1 814	48.15 Mo
Mai 2013	129	321	814	1 553	47.85 Mo
Juin 2013	119	294	852	1 532	49.40 Mo
Juil 2013	123	288	737	1 493	42.20 Mo
Aoû 2013	137	307	901	1 787	70.58 Mo
Sep 2013	113	276	898	1 623	60.01 Mo
Oct 2013	157	387	1 357	2 694	109.00 Mo
Nov 2013	117	352	1 076	1 774	58.69 Mo
Déc 2013	148	456	1 431	2 527	87.22 Mo
Total	1 542	3 933	12 195	22 085	702.03 Mo

The 2013 traffic on CESAR public website analysed by CEA tool.

Several interesting facts can be highlighted:

- on week days, there is an average of 7,5 individual visits per day.
- the main visited pages are : *home*, *description of WP2* and *WP3* (elementary components and complex circuits) and the general "*applications*" page.

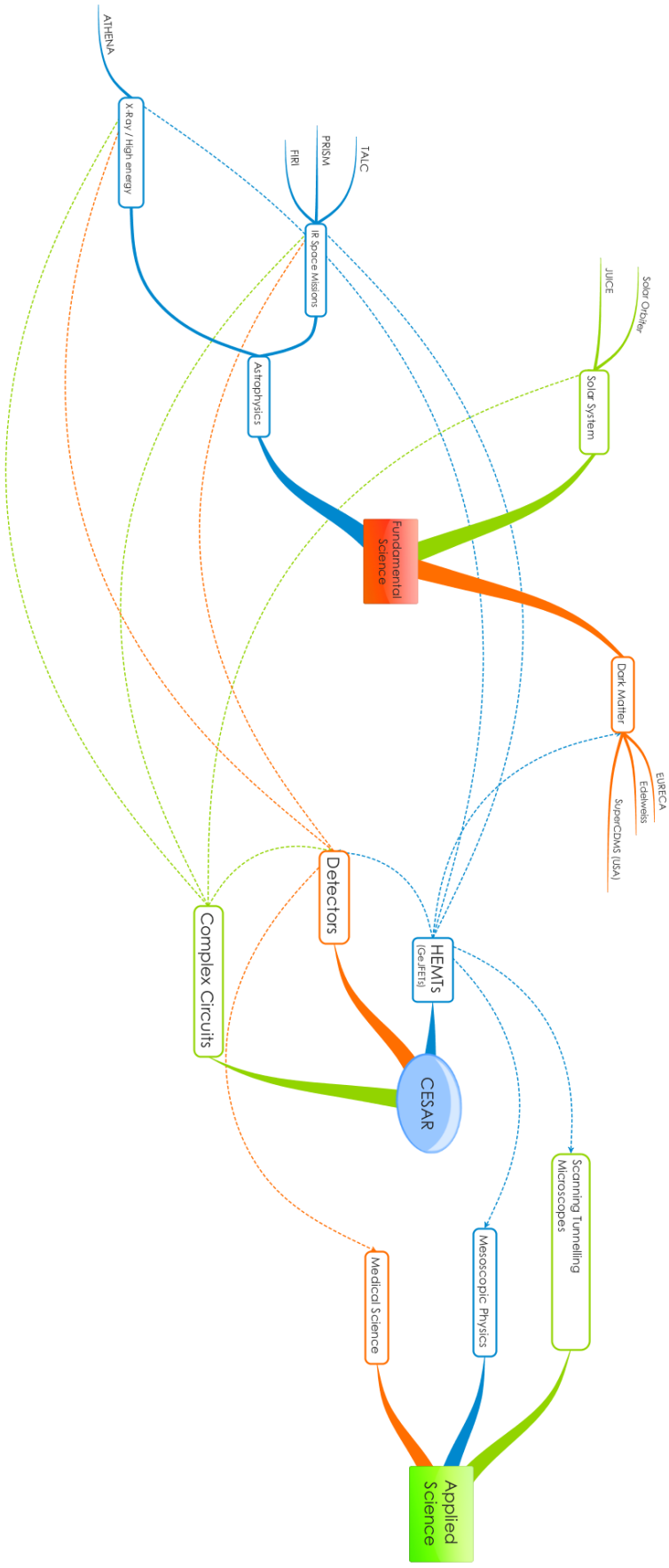
- visits per country : mainly Europe (France, Italy, Germany, UK), Russia, China and USA.
- The majority of the visitors come to the site through Google, by typing the following keywords: "*cryogenic electronics*", "*electronics in space*" or "*space applications*". We can see for example that by typing "*cryogenic electronics*" in Google, the CESAR page rises at an average position of 1.4 (statistics established over a period of one year).

The internal and private CESAR website is also up and running. It is used only for reports depository and archives.

The two CESAR websites will continue to be operational and maintained by CEA for at least 2 years after the end of CESAR.

6.2 Exploitation

The fields for exploitation in the CESAR framework have been described in the **Deliverable 6.2**. For most of these domains (X-ray astrophysics, Far-Infrared / submillimeter astrophysics, mesoscopic physics, Dark Matter search), detailed studies are on-going on the potential use of CESAR work, in particular, concerning the European Dark Matter Search experiment Eureca (see for example the paper "**EURECA Conceptual Design Report**", G. Angloher et al, Physics of the Dark Universe, Vol. 3, April 2014, pp 41-74). Figure 2 summarizes the different exploitation fields and the inter-connections between the different CESAR themes.
The good results that have been obtained during the project (HEMTs, cryogenic read-out technology, Magnetometry, X-Ray and Sub-mm detectors) put the different CESAR groups in good position for the selection of the next ESA astrophysics missions (PRISM/CoRE+, JUICE).



Fields of exploitation for CESAR.

6.3 Dissemination

The main event related to CESAR activities during the project duration was the **WOLTE10** workshop organized in Paris, mainly by persons coming from several CESAR Institutes (see the dedicated **deliverable 6.5**).
Two **training sessions** were organized during the project, see **deliverable 6.3**.
Several **articles, conference proceedings and talks** in scientific schools, linked to CESAR were produced during the project.

Published :

- **Q. Dong**, Y. X. Liang, D. Ferry, A. Cavanna, U. Gennser, L. Couraud, and Y. Jin, « Ultra-low noise high electron mobility transistors for high impedance and low frequency deep cryogenic readout electronics» **, Appl. Phys. Letters**, **105**, 013504 (2014).

- **V. Revéret et al**, "CESAR: Cryogenic Electronics for Space Applications", J Low Temp Phys, Online Edition (2013)

- **S. Jezouin,** F. Parmentier, A. Anthore, U. Gennser, A. Cavanna, Y. Jin, F. Pierre « Quantum limit of heat flow across a single electronic channel » ***Science*** **342**, 601 (2013)

- **Q. Dong et al**, "The role of the gate geometry for cryogenic HEMTs: towards an input voltage noise below 0.5 nV/Hz$^{1/2}$ at 1 kHz and 4.2K", J Low Temp Phys, 167, 626-631 (2012)

- **Y.X. Liang et al**, "Input noise voltage below 1 nV/Hz$^{1/2}$ at 1 kHz in the HEMTs at 4.2 K", J Low Temp Phys, 167, 632-637 (2012)

- **Y. X. Liang et al**, "Insight into low frequency noise induced by gate leakage current in AlGaAs/GaAs high electron mobility transistors at 4.2K", Appl. Phys. Lett. 99, 113505 (2011)

- Francesca Chiodi, Cyrille Gardes, Geraldine Hallais, Daniel Bouchier, Dominique Debarre, " *Ohmic contacts in metal/n-type Ge junctions made by laser processing*" 10th International Workshop On Low Temperatures Electronics (WOLTE 10) October 14-17, 2013 Paris, France

Submitted :

- **Francesca Chiodi** *et al*, submitted to J. Appl. Phys 2014.

- Some papers will be presented at **LTD16** conference (Low Temperature Detectors) in Grenoble in 2015.

Finally, it must be noted that **CESAR** has been pre-selected for the **2014 Edition of the "Etoiles de l'Europe" Prize by the French Ministry of Research**.

7 Conclusion

We are now at the end of the CESAR_SPACE Project. This document shows the progress done in the cryogenic electronics field by the CESAR laboratory network during these three years. All this work is meaningless if we cannot put it in the prospective of new developments. New developments can be as well direct applications to space instruments, or follow on of the different themes developed in CESAR, or even new developments made possible by the products of our Project. It is time now to look forward and replace this work in a prospective for future applications.

Single elements.
During the last "Astronomy and instrumentation" SPIE Conference, few weeks ago, the importance for Cosmological Microwave Background (CMB) Experiments of the first readout stage became obvious when dealing with thousands of detectors. The faraway Si JFETs are no longer compatible with the experimental setup. Transistors must be located as close as possible of the detector arrays, at kelvin or sub-kelvin temperature. The polarization measurement level required by the detection limits is hampered by the noise (mainly the 1/f side) of the HEMTs manufactured overseas.
The HEMTs developed by CNRS/LPN are already advertised for Dark matter search, and were delivered to the CDMS (US) and Edelweiss (Fr) experiments. We expect these applications (independent from CESAR) will demonstrate to a wider scientific community their intrinsic qualities.
GeJFETs is a grail for more than 20 years in cryogenic electronics. A new manufacturing process is tested in the CESAR Project context. We have not succeeded yet, but very interesting by-products (GUILD contacts) are already used in the microelectronics manufacture platform at CNRS/IEF.

Complex circuits.
The complex circuits developed in the different CESAR applications (X-Ray micro-calorimeter, Far Infrared bolometer arrays and Vector Magnetometry), for readout and signal processing at the cold stage, can have direct applications for future spaces projects.
ATHENA(+) is the second large program of ESA in the 2020's. The cold circuits developed by CEA/SEDI for X ray Calorimeters can solve many system issues related to the global sensitivity requirements. This is still very dependent of the type of sensors used for the final detectors.

As said previously, and beyond the Far IR field, the cryogenic circuit developed in the Project can advantageously be used in space for B_MODES detection in the CMB. This topic had recently received a large echo in the Press. Are gravitational waves imprinted in the CMB polarization picture? The detection by BICEP2 at the South Pole observatory is today widely debated. We are confident that a new observatory will be selected either by NASA after the success of WMAP or by ESA after Planck remarkable scientific return. The kind of electronics we have built, in the CESAR context, will be considered at a very general level, because risks on signal degradation can be avoided. This also widely

reduces some high level system constraints at the cost of a more sophisticated cryogenic system.

The application to magnetic measurements for planetology is a very interesting case. Despite the ultimate sensor exists for many years now: the Superconducting Quantum Interference Device, its use as an array or in space conditions is not straightforward either because it must be maintained at ~4 kelvins or because the very low impedance of the sensor itself. A good compromise is the Giant Magnetoresistance devices. It can be operated at warmer temperatures, it is a resistive sensor (well adapted to usual electronic circuits), and approaches performance requirements sufficient for many space applications. The CESAR developments show that the association GMR plus cryo-electronics pushes the performance of a 3D device (vector) at an unprecedented sensitivity level for this type of sensor.