VHiSSI

Very High Speed Serial Interfaces

Final Publishable Summary Report

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STAR-Dundee

RAMONchips

ACE ic
ASIC Design House

AIRBUS
DEFENCE & SPACE

innovations
for high
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microelectronics

Leibniz-Institut für
innovative Mikroelektronik

The research leading to these results has received funding from the European Union Seventh Framework Program (*FP7/2007-2013*) under grant agreement no. 284389

1 EXECUTIVE SUMMARY

Several important future space-based instruments, for example synthetic aperture radar (SAR) and hyper-spectral imagers will be capable of producing data at data rates of several Gbits/s. New downlink telemetry techniques (laser and Ka-band communications) will be able to provide much higher downlink capacity than previously possible. High-speed memory technologies will be able to serve multiple high data-rate instruments and stream data to ground on demand. To support the growing need for onboard communications network bandwidth high-speed serial interfaces are necessary. The Very High Speed Serial Interface (VHiSSI) project has researched and designed an experimental high-speed serial interface chip to support spaceflight applications. This chip implements the emerging ESA SpaceFibre standard serial communications protocol and includes important quality of service (QoS) and fault detection, isolation and recovery (FDIR) capabilities. It was implemented in a new radiation tolerant chip technology and manufactured by a European foundry and tested extensively. The VHiSSI research programme has researched, designed and developed an experimental high speed serial interface chip, VHiSSI, which:

- Provides multi-Gbit/s serial data-link technology, essential for future spacecraft onboard data-handling systems.
- Levers prior and concurrent research on the emerging SpaceFibre standard, to provide a complete multi-Gbit/s serial technology for spacecraft onboard data-links and networks, including fault detection, isolation and recovery (FDIR) and quality of service (QoS).
- Provides a versatile chip architecture, which can be adapted and configured to support multiple applications.
- Provides the critical clock-data recovery mechanism on existing European chip technology.
- Uses a European semiconductor fabrication facility, enhancing and developing its capabilities for radiation tolerant chip design and production with a radiation tolerant library. Further work needs to be done related to the radiation single event effects (SEE).
- Provides a non-dependent technology allowing unrestricted use on European spacecraft and substantial export opportunities - an important capability for Europe.

The principal benefits of the VHiSSI research programme are:

- Very high-speed serial-interface technology applicable to many space missions, including large and small satellites, robotic missions, planetary landers and rovers, launchers and related electronic test equipment, and which is capable of spin-out to a wide range of terrestrial applications, including demanding robotics applications.
- A high-speed serial interface chip implemented using a radiation-hard standard cell library optimized for a new 130 nm CMOS process, although further work needs to be carried out related to radiation single event effects (SEE).
- Mixed-signal high-speed radiation-hardened integrated circuits that are free from international export restrictions (non-dependent) that are fabricated and tested in Europe, and that are available to members of the European Union for use in space missions. The SEE issue detected in the last month of the project needs to be addressed and space grade qualification is necessary.

The medium term impact of the VHiSSI programme will be an independent European technology for spacecraft high-speed data-links and network technology. The VHiSSI research will lead to a complete spacecraft onboard data-handling solution, saving mass and power, improving reliability, and substantially simplifying complex system design.

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2 Project Context and Objectives

2.1 Context

Space-based Earth observation and scientific instrumentation currently under development will push the limits of on-board data-handling technology. In the past Mil-Std 1553 and proprietary data-links were used to get instrument data from the instruments to the on-board mass memory unit and to the down-link telemetry system. Over the past decade the proprietary data links have been replaced with a standard networking technology designed for use on-board spacecraft: SpaceWire. While SpaceWire is currently being used to fulfil the on-board data-handling requirements of many missions, there are some very high data-rate instruments which are beyond its capabilities.

Several important future space-based instruments, for example synthetic aperture radar (SAR) and hyper-spectral imagers will be capable of producing data at data rates of several Gbits/s. New downlink telemetry techniques (laser and Ka-band communications) will be able to provide much higher downlink capacity than previously possible. High-speed memory technologies will be able to serve multiple high data-rate instruments and stream data to ground on demand. To support the growing need for onboard communications network bandwidth, technologies able to support multi-Gbits/s data transfer have been developed, e.g. Channel Link and, Wizard Link. Unfortunately these are all restricted USA devices resulting in a critical European dependency.

SpaceFibre is a spacecraft onboard data-link and network technology being developed by University of Dundee for the European Space Agency (ESA) which runs over both copper and fibre optic cables. Initially targeted at very high data rate instruments like Synthetic Aperture Radar (SAR) and multi-spectral imaging instruments, SpaceFibre is capable of fulfilling a wider set of spacecraft onboard communications applications because of its inbuilt QoS and FDIR capabilities and its backwards compatibility with the ubiquitous SpaceWire technology.

SpaceFibre operates at 2.5 Gbits/s providing 12 times the throughput of a SpaceWire link with current flight qualified technology and allowing data from multiple SpaceWire devices to be concentrated over a single SpaceFibre link. This substantially reduces cable harness mass and simplifies redundancy strategies. The innovative QoS mechanism in SpaceFibre provides concurrent bandwidth reservation, priority and scheduled QoS. This simplifies spacecraft system engineering through integrated quality of service (QoS), which reduces system engineering costs and streamlines integration and test. Novel integrated FDIR support provides galvanic isolation, transparent recovery from transient errors, error containment in virtual channels and frames and “Babbling Idiot” protection. SpaceFibre enhances onboard network robustness through its inherent FDIR and graceful degradation techniques incorporated in the network hardware. This simplifies system FDIR software, reducing development and system validation time and cost. SpaceFibre includes low latency event signalling and time distribution with broadcast messages enabling a single network to be used for very high data rate payload data, carrying SpaceWire traffic, deterministic information for command/control, time distribution and event signalling.

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SpaceFibre is backwards compatible with existing SpaceWire equipment at the packet level allowing simple interconnection of SpaceWire devices into a SpaceFibre network and enabling that equipment to take advantage of the QoS and FDIR capabilities of SpaceFibre.

Present implementations of SpaceFibre using separate SerDes and FPGA devices are dependent on USA components.

2.2 Project Objectives

The primary motivation for the proposed VHiSSI project was to provide Europe with important very high-speed serial interface technologies, enhancing the technical capabilities and overall competitiveness of the European space industry, enabling it to compete effectively on the world market.

The VHiSSI research programme has the following key objectives:

- A justified set of requirements and use cases for the VHiSSI chip, which takes into account requirements from spacecraft primes and equipment manufacturers, across the EU.
- A consolidated concept and architectural design, which takes into account relevant literature and concurrent research and technology development work on the SpaceFibre standard and applications, explores and analyses alternative designs, and trades-off alternative solutions.
- A detailed specification for the VHiSSI chip, based on the requirements and use cases and the conceptual design and analysis work.
- A design for the digital part of the VHiSSI chip implemented in an FPGA and validated against the requirements and use cases.
- A radiation tolerant design of the VHiSSI chip using a European foundry.
- A design of the high-speed SerDes component including clock recovery and drivers/receivers targeted for the process available from the European foundry.
- An implementation of the experimental VHiSSI chip, packaged ready for experimentation and testing.
- Characterisation of the functionality, performance and radiation tolerance of the VHiSSI chip.
- System level validation of the VHiSSI chip against the requirements and flight representative use cases.
- Disseminated results of the VHiSSI research programme to the ESA, European space industries, and to the international space community.
- An exploitation plan covering the development of flight grade chips, and an appropriate market strategy including support to European space missions, and export opportunities.

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2.3 Project Team

To achieve these goals, technological spin-in from the European microelectronics research community and multi-lateral collaboration between leading European institutions and industry, both large prime contractors and SMEs, was essential to provide the necessary breadth of technical knowledge, capability and experience. A highly experience team of European academic and industrial organisations was assembled for the VHiSSI project:

The University of Dundee (UNIVDUN) has long experience in spacecraft onboard network technology, writing the SpaceWire standard with support from the European Space Agency (ESA) and input from engineers across Europe. UNIVDUN has extensive experience in related IP core design having designed SpaceWire interface, remote memory access protocol (RMAP) and router cores for ESA, JAXA and other organisations.

The principal responsibilities of UNIVDUN were overall project management, initial requirements and use cases (in conjunction with Airbus DS), devising the architectural concepts and specification, designing an independent test bench for the VHiSSI chip and, in conjunction with STAR-Dundee, functional and performance characterisation and system level testing of the VHiSSI chip.

Airbus DS GmbH is a major international spacecraft manufacturer that undertakes system integration and also designs and manufactures spacecraft payloads.

The principal responsibilities of Airbus were the requirements and use cases for VHiSSI based on their extensive spacecraft design experience and the functional characterisation of the VHiSSI chip in Total Ionising Dose (TID) and heavy ion characterisation for Single Event Effects.

STAR-Dundee Ltd is a world leading supplier of SpaceWire IP cores and test and development equipment. STAR-Dundee specialises in spacecraft on-board data-handling systems and the IP cores and test and development equipment needed to successfully realise these systems.

The principal responsibilities of STAR were the design, simulation and FPGA-based validation of the VHiSSI VHDL core, the design and manufacture of the VHiSSI test boards, and, in conjunction with UNIVDUN, functional and performance

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characterisation and system level testing of the VHiSSI chip.

ACE-IC Ltd is a fabless Analog-Mixed Signal design house specializing in design applications for the Communication industry, in particular the next generation of rapid information transfer applications. ACE-IC has expertise in designing Multi-rate SerDes (from 1Gbps up to 12Gbps) which supports several tele/data communication protocols.

The principal responsibilities of ACE-IC were the design of a radiation tolerant, high-speed SerDes for the VHiSSI chip.

RAMON CHIPS Ltd. is a fabless semiconductor company focused on developing unique VLSI /ASIC solutions for space applications. RAMON has expertise in designing digital and analogue radiation-hardened chips from specifications, synthesis of functions and algorithms into robust radiation-tolerant cores, and converting FPGA designs into radiation-hardened ASICs.

The principal responsibilities of RAMON were the definition of the test and validation plan for the experimental ASIC, and design of the experimental ASIC and the RadHard libraries.

IHP carries out research and development in the area of microelectronics and information technology. IHP's core competences are in materials research, semiconductor technology, RF-circuit design and system development in a closed innovation chain. The IHP pilot line provides production facilities for internal projects but can also be used by third parties through MPW & prototyping services.

The principal responsibilities of IHP were manufacturing and supporting the testing of the VHiSSI chip, development of the advanced and nonstandard rad-hard cells and improvements to the rad-hard design flow.

Synergie-Cad Instruments srl (SCI) is an Italian company dedicated to providing testing services to semiconductor companies and fabless.

The principal responsibilities of SCI were load board schematics development, test program development, test program and load board debug.

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3 Main Scientific and Technological Results

3.1 Project Overview

An overview of the project is illustrated in Figure 3-1. There are seven technical work packages, one specifically looking at exploitation, and a management work package.

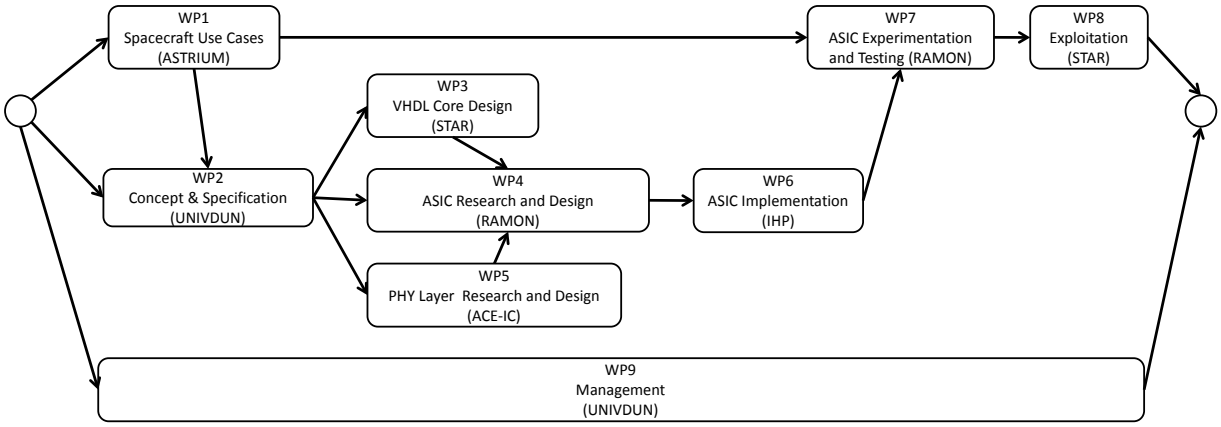

Figure 3-1 Overall strategy of the work plan

The research began with WP1 (Spacecraft Use Cases) where a comprehensive set of requirements for the experimental VHiSSI chip were gathered from the European spacecraft engineering community by Airbus DS GmbH, focusing on a small device which could be used to provide very high-speed data-links on-board a spacecraft. A set of uses cases for VHSSI were also devised taking into account information from spacecraft prime and equipment manufacturers across Europe. From the use cases a corresponding set of test scenarios were derived for use in the system level validation of the VHSSI.

WP2 (Concepts and Specification) provided the overall architectural concept for VHSSI. Research on the system architecture examined the potential use of VHSSI in high-speed networking onboard future spacecraft. The functional, performance and interface specifications for the VHSSI chip were derived from the requirements produced in WP1. A versatile chip interface was designed by University of Dundee which covers many potential applications while keeping the number of pins required on the chip to a minimum.

WP3 (VHDL Core Design) focused on the digital design for the VHSSI chip which was carried out by STAR-Dundee Ltd. The VHDL RTL code for the VHSSI chip was designed based on the specifications developed in WP2. Following successful simulation and testing, an FPGA implementation of VHiSSI was produced and used to perform extensive system-level experimentation and validation based on the test scenarios devised in WP1 in preparation for the backend ASIC design tasks in WP4.

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WP4 (ASIC Research and Design) covered the research and development of radiation-tolerant, high-speed circuits suitable for manufacturing on the IHP European foundry. The use of the IHP chip foundry required a complete radiation tolerant component library to be designed. The design was based on RadSafeTM libraries, developed by Ramon Chips, and ported to the IHP 0.13u process. It utilizes several Radiation Hardening By Design (RHBD) techniques, which provides high immunity to all radiation effects. The libraries included standard cells, IO cells including LVDS buffers, and SRAMs with complementary EDAC logic for enhanced soft error protection.The library test components from Ramon Chips were implemented in the RADIC 5 test chip and validated. Some small improvements were made to the library for the VHiSSI device. The VHiSSI chip logic design from STAR-Dundee Ltd (WP3) and the improved SerDes from ACE-IC (WP5) was designed into the IHP chip technology by Ramon Chips including floor planning, place and route, and timing extraction. STAR-Dundee Ltd supported this activity carrying out static timing analysis of the placed and routed design. The chip was then manufactured by IHP on its 130 nm Bi-CMOS process (WP6).

In WP5 (PHY Layer Research and Design) the serialiser/deserialiser, clock-data recovery circuitry and the high-speed serial driver/receiver technology (SerDes) was carried out by ACE-IC. This was a particularly demanding design activity due to the speed of the interface and the required radiation tolerance. The SerDes core, which was designed by ACE-IC, was based on guidelines provided by Ramon Chips for hardening against radiation effects. The design of the SerDes was tested in the RADIC5 test chip and various improvements subsequently made for the VHiSSI chip. The output of WP5 fed into the chip design of WP4.

In WP6 (ASIC Implementation) first the RADIC5 test chip and then the experimental VHiSSI chip were implemented on the 130 nm European chip technology from IHP. The resulting VHiSSI chip is shown in Figure 3-2.

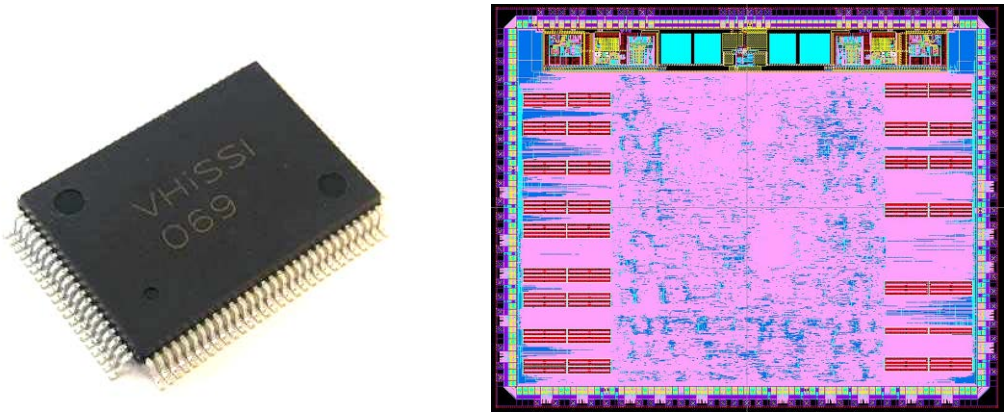

Figure 3-2 VHiSSI SpaceFibre Chip

In WP7 (ASIC Experimentation and Testing) the VHiSSI chip was extensively evaluated. While the chip was being manufactured in WP6, SCI, IHP and STAR-Dundee Ltd developed test vectors for chip testing and STAR-Dundee Ltd designed, implemented and tested four test boards for the VHiSSI chip covering different functions. VHiSSI chip was encapsulated into a plastic package and initial chip testing carried out on a chip tester at IHP. The chips that passed these tests were then used by

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STAR-Dundee Ltd, University of Dundee and ACE-IC for the functional and performance testing (see Figure 3-3). Experiments were conducted to assess many aspects of the device including: functionality, performance and system level validation.

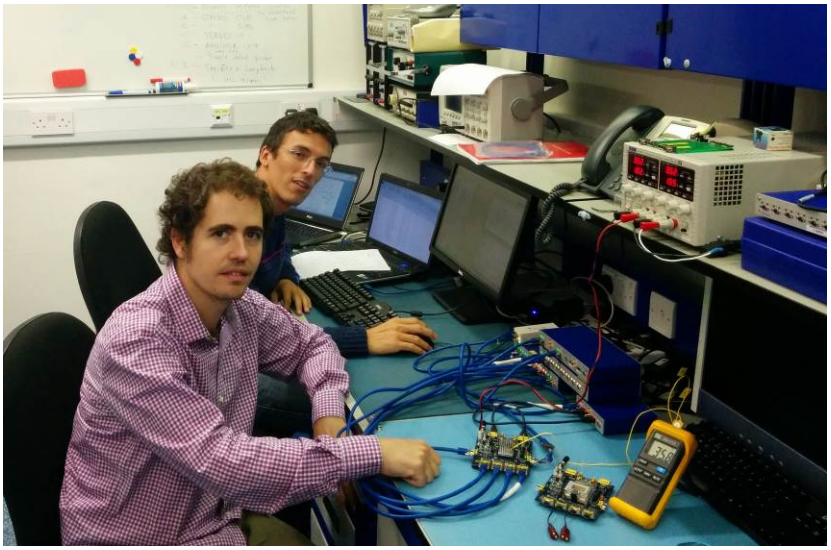

Figure 3-3 Testing the VHiSSI SpaceFibre and SpaceWire Interfaces

Throughout the programme of work presentations were made to the international SpaceWire Working Group and to relevant conferences to ensure engagement with the broader spacecraft onboard networking and data link community. WP8 (Exploitation and Dissemination) focused on this dissemination and the formulation of an exploitation plan.

WP9 ran in parallel with all the other work packages to provide efficient and effective management of the project. Overall project management was carried out by an experienced management team at UNIVDUN.

The results of each work package will now be described in more detail.

3.2 WP1 Spacecraft High Speed Serial Interface Use Cases

An initial set of requirements and use cases were developed for the VHiSSI chip taking into account the needs of European aerospace industry. The initial requirements and use cases were presented to the 18th International SpaceWire Working Group meeting in April 2012, by Paul Rastetter of Astrium. This formed the starting point of a more general presentation on SpaceFibre technology, which also included an overview of the VHiSSI aims and outline chip concept. Informal feedback from various SpaceWire working group members was very positive. At the SpaceWire Interagency Meeting on 25th April, support was provided for the SpaceFibre concept from all parties, including ESA, NASA, JAXA and RosCosmos, with several groups interested in conducting parallel prototyping activities.

The primary applications envisaged for the VHiSSI chip are listed below:

- SpaceWire to SpaceFibre Bridge i.e. harness mass and power reduction and longer distance communication.

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- Instrument to Mass Memory or Processor
- Mass memory from Instruments
- Mass Memory to Downlink Telemetry
- Downlink Telemetry from Mass Memory.
- Control Processor controlling instruments and other units
- Data Processor Array
- Integrated Avionics Network
- Long distance control connection for launcher using Fibre Optics.
- VHiSSI Chip Applications

Several important use cases for the VHiSSI chip are considered in the following subsections.

3.2.1 High Data-Rate Instrument Interface

SpaceFibre offers substantially higher data rates than SpaceWire to support high data-rate instruments. Connection of a high data-rate instrument to a mass memory unit via SpaceFibre is illustrated in Figure 3-4.

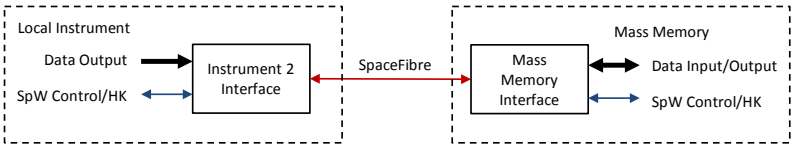

Figure 3-4 High Data-Rate Instrument Connected To Mass Memory

To provide data at high-speed from a local instrument to the SpaceFibre interface a parallel interface is required. To operate with current space qualified FPGAs this interface has to be 32 bits wide, which requires a 62.5 MHz interface clock (32-bits x 62.5 MHz = 2 Gbits/s, which after 8B/10B encoding is 2.5 Gbits/s signalling rate).

The simplest type of interface is a FIFO type interface, which is straightforward to connect to an FPGA. For high data rate transfer from an instrument it is only necessary to write data to an output VC buffer in the SpaceFibre interface. A slower speed interface, e.g. SpaceWire, would be useful for controlling and reading housekeeping information from the instrument.

If the instrument includes an embedded processor it may be preferable to use a memory type interface to write and read data from the SpaceFibre VC buffers in the SpaceFibre interface. This interface can then also be used to access the configuration, control and status registers inside the SpaceFibre interface. In this case it is the responsibility of the instrument to handle the transfer of data to the SpaceFibre interface.

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A DMA controller included in the SpaceFibre interface transfers responsibility for data transfer from the instrument controller to the SpaceFibre interface. This may save some important processing power within the instrument controller.

The VHiSSI device is able to provide a SpaceFibre interface for high data rate instruments using a FIFO, memory or DMA type interface to an FPGA or processor. This interface is designed to be able to operate at clock speeds achievable by flight qualified FPGAs while sustaining 2 Gbits/s data transfers. It also is designed to minimise the number of pins required for the interface.

3.2.2 SpaceWire to SpaceFibre Bridge

SpaceWire has been used extensively to provide a standard interface to various instruments. To connect these instruments into a SpaceFibre based data-handling network a SpaceWire to SpaceFibre Bridge is required.

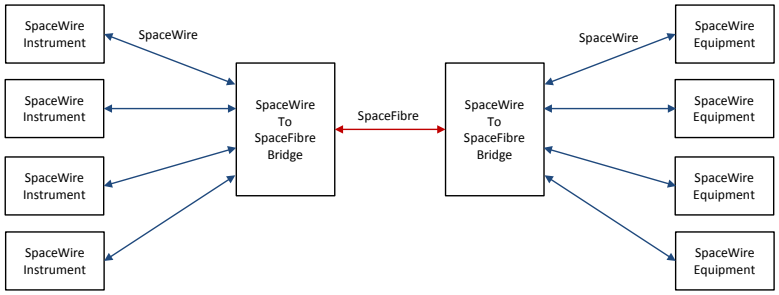

Figure 3-5 SpaceWire to SpaceFibre Bridge

Figure 3-5 shows a SpaceWire to SpaceFibre Bridge being used to multiplex several SpaceWire links over a single SpaceFibre link. In this particular example four instruments with SpaceWire interfaces are connected to some other SpaceWire enabled equipment. Bridging between SpaceWire and SpaceFibre is straightforward since both protocols use the same packet format.

The VHiSSI chip can operate as a SpaceWire to SpaceFibre bridge with either LVDS or LVTTL SpaceWire interfaces and includes an internal SpaceWire router.

3.2.3 Mass Memory Interface

A mass memory requires several SpaceFibre interface connections to support several high data-rate instruments and instruments with SpaceWire interfaces. This is illustrated in Figure 3-6.

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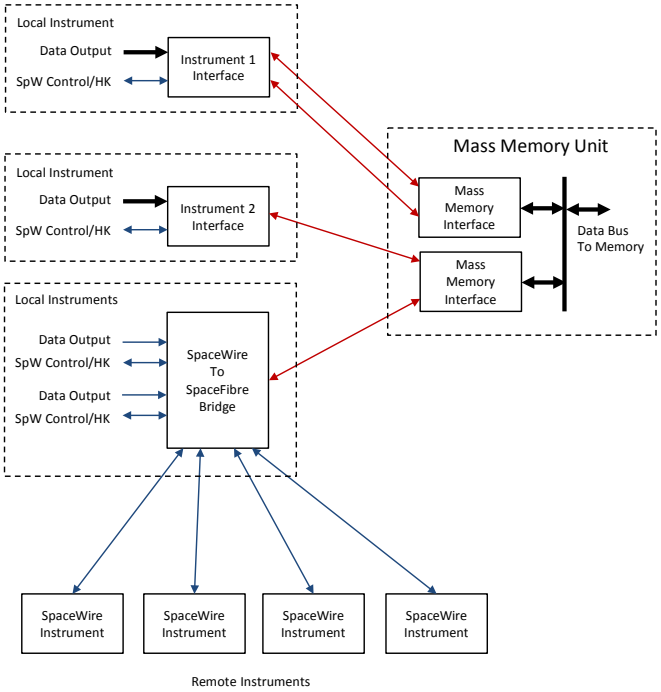

Figure 3-6 Mass Memory Interface

Two high data-rate instruments are shown, one with a single SpaceFibre link and the other requiring two SpaceFibre links to support data rates of 4 Gbits/s. Several SpaceWire instruments are also connected to the mass memory via a SpaceWire to SpaceFibre Bridge.

The Mass Memory unit provides four SpaceFibre interfaces connected to a common bus or network for accessing the memory modules that are to store the data.

The VHiSSI chip can provide all the SpaceFibre interfaces required in the example network of Figure 3-5: high-speed instrument interfaces, SpaceWire to SpaceFibre bridge and the interface to the mass memory unit.

3.2.4 Control Processor

Configuration and control information can be sent over a SpaceFibre network using individual virtual channels or a virtual network. A SpaceFibre router allows a control processor to access all the instruments and other equipment on the network as illustrated in Figure 3-7.

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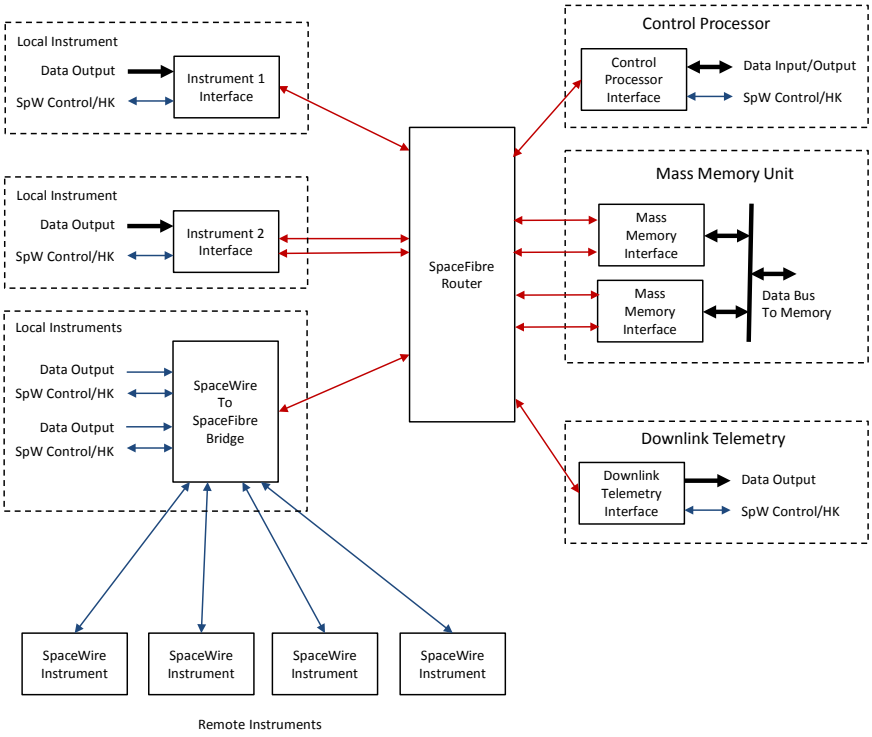

Figure 3-7 Control Processor on SpaceFibre Network

Figure 3-7 shows a complete SpaceFibre based on-board data-handling system. A SpaceFibre router is used to interconnect the various units. A control processor is connected to this router. It is able to send configuration, control and status request commands to all of the other units on the network. Typically a virtual network would be used to manage this control and status information, where one virtual channel in each unit is dedicated to control/status and each of them is given the same virtual channel number, e.g. VC0. The control processor then sends SpaceWire packets containing commands over VC0 to another unit. This unit responds over VC0. Since the control processor is the master of the VC0 virtual network, there is no undesirable contention between SpaceWire packets on VC0. This approach leaves all the other virtual channels available for data transfer.

The SpaceWire instruments do not support virtual channels, so control/status packets and data packets have to be multiplexed over the SpaceWire links. The SpaceWire to SpaceFibre Bridge must be able to support this multiplexing of SpaceWire packets containing control information, status or instrument data. This requires a SpaceWire router which could be provided within the SpaceWire to SpaceFibre Bridge. Normally configuration, control and housekeeping requests require small packets and should therefore not have a major impact on data transfer over the single SpaceWire link from instrument to the SpaceWire router in the SpaceWire to SpaceFibre Bridge.

The VHiSSI device together with a SpaceFibre router device can provide all the SpaceFibre network functionality needed for onboard data-handling architectures like that of Figure 3-7.

3.3 WP2 Concepts and Specification Development

The overall architectural block diagram of the VHiSSI chip is illustrated in Figure 3-8.

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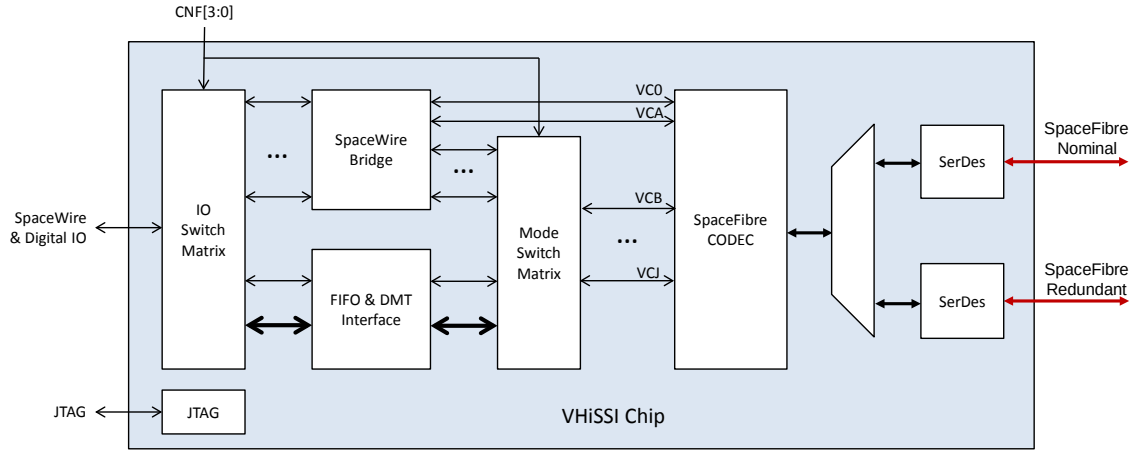

Figure 3-8 VHiSSI Overall Architecture

There are five main functions within the VHiSSI chip:

- SpaceWire Bridge
- FIFO, DMA, Memory and Transaction Interface
- SpaceFibre Interface
- SerDes
- IO Switch Matrix
- Mode Switch Matrix

The SpaceWire Bridge provides a bridge between SpaceWire and SpaceFibre with up to 11 SpaceWire interfaces being available. The SpaceWire Bridge includes a SpaceWire router which allows routing between SpaceWire ports and Virtual Channel (VC) buffers of the two SpaceFibre interfaces. Configuration of the VHiSSI chip can be carried out over any SpaceWire interface connected to the embedded SpaceWire router or over VC0 or VC1 of the SpaceFibre interface. The SpaceWire Bridge is connected to the IO Switch Matrix and to the Mode Switch Matrix.

The FIFO and DMA, Memory and Transaction (DMT) Interface provides various types of parallel interface into the VHiSSI chip for sending and receiving data over the SpaceFibre interfaces. The various parallel interface functions have been designed with specific application scenarios in mind and between them are able to operate with many types of local host system, including FPGAs and processors. The parallel interface is also designed to use a small number of pins, so that the VHiSSI chip can fit into a small (100 pin) package. The FIFO mode provides a direct parallel interface to two SpaceFibre virtual channels. The memory type interface provides a 32-bit bus interface for accessing VHiSSI registers or VC buffers. It is a multiplexed address/data bus, with the VHiSSI device providing an internal address latch/counter to hold the register/VC buffer address. The transaction interface is similar to the memory interface, but aims to simplify software interfacing. A single address line is used to distinguish commands and status information from data. A command is written to the VHiSSI device to specify the transaction that is about to take place. For data transfer to/from a VC buffer, a

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read of status information provides the status of the VC buffer identified in the command. The data transfer can then take place in a burst transfer the maximum size of which is determined by the VC buffer status information. The DMA interface puts the VHiSSI chip in control of data transfers. When there is data ready to transfer, an internal DMA controller in the VHiSSI device requests control of the external data bus. Once granted it then affects the data transfer. An external address latch/counter is required, which may be implemented in an FPGA. The FIFO and DMT interface is connected to the IO Switch Matrix and to the Mode Switch Matrix. On reset the IO pins and connections to the VC buffers from the FIFO and DMT interface and SpaceWire Bridge are determined and set by these two switch matrices.

The SpaceFibre Interface has 11 virtual channels. VC 0 is intended primarily for VHiSSI device and local system configuration and monitoring and is connected to the embedded SpaceWire router. VC1 is connected to the embedded SpaceWire router. The other VCs are either connected to the SpaceWire router, directly to a SpaceWire interface, or to the parallel interface, depending on the mode of operation. Each VC supports full SpaceFibre QoS which can be configured independently for each VC. VC0 and VC1 are directly connected to the embedded SpaceWire router. The other SpaceFibre VC buffers are connected to the Mode Switch Matrix which connects them to either the SpaceWire Bridge or the parallel interface. The other side of the SpaceFibre interface is connected via a multiplexer to either the nominal or redundant SerDes and CML transceiver.

The SerDes converts parallel data words from the SpaceFibre interface into a serial bit stream and vice versa. On the receive side the bit clock is recovered from the serial bit stream by the SerDes. The SerDes includes integral CML transceivers.

The IO Switch Matrix connects either the SpaceWire LVDS, SpaceWire LVTTL or parallel interface signals from the FIFO and DMT interface to the digital IO pins of the VHiSSI chip. Configuration is static and determined on exit from device reset, i.e. on the rising edge of the RSTN signal.

The Mode Switch Matrix connects either the SpaceWire Bridge or FIFO and DMT interface (parallel interface) to the VC buffers of the two SpaceFibre interfaces. Configuration is static and determined on exit from device reset, i.e. on the rising edge of the RSTN signal.

In addition to these major functions the VHiSSI chip includes a JTAG test port and some other device test modes.

The architecture of the VHiSSI chip was translated into a detailed specification for the VHDL code, which was then implemented in WP3.

3.4 WP3 VHiSSI VHDL Core Design

3.4.1 VHDL Coding

In WP3 the VHDL code for the VHiSSI chip was implemented by STAR-Dundee. A test bench for the VHiSSI VHDL code was designed by UNIVDUN. STAR and UNIVDUN then carried out simulation and

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testing of the VHiSSI VHDL code using the test bench. The VHDL code was then implemented in an FPGA and tested using a specially designed test board.

3.4.2 VHiSSI FPGA Test Board

A test board was designed, manufactured and tested containing an FPGA into which the VHiSSI design could be programmed (see Figure 3-9). The VHiSSI VHDL code was placed and routed for the FPGA on the test board and post layout simulation carried out to check that the place and routing had not introduced any errors. The VHiSSI design was then loaded into the FPGA test board and initial testing was then carried out. Functional validation against the requirements from WP1 was then performed and system level validation done for the SpaceWire to SpaceFibre bridge mode and parallel interface mode. The resulting VHiSSI VHDL code was extensively tested ready for ASIC implementation.

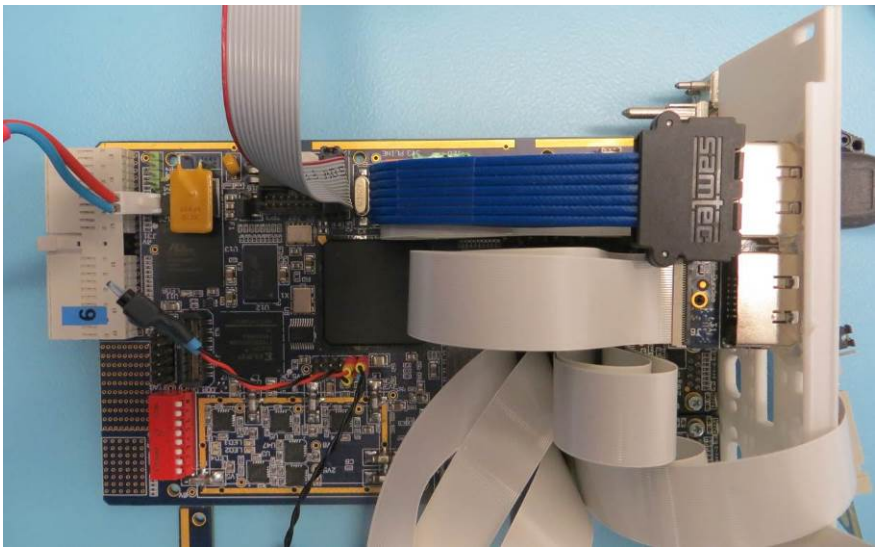

Figure 3-9 VHiSSI FPGA Test Board

3.4.3 SpaceWire-SpaceFibre Bridge Mode Validation

The validation of VHiSSI as a SpaceWire-SpaceFibre bridge was carried out using a SpaceFibre interface unit (STAR Fire) to generate SpaceFibre packets (see Figure 3-10). This setup tested the bridging from SpaceFibre to SpaceWire and from SpaceWire to SpaceFibre. The VHiSSI FPGA implementation passed all the tests for this mode of operation.

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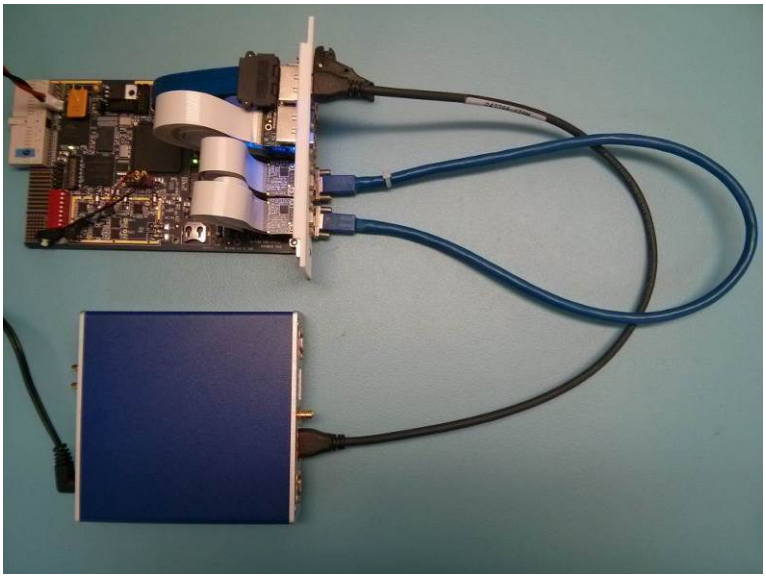

Figure 3-10 Photograph of SpaceWire to SpaceFibre Bridge Test Setup

3.4.4 Parallel Interface Mode Validation

To test the VHiSSI FPGA in the FIFO mode of operation two VHiSSI FPGA test boards were used (see Figure 3-11); one programmed as a VHiSSI chip and the other as a tester board. A script file (which was also used during VHDLS simulation testing) was used to define the tests to be executed by the tester. Two test scripts were created: one containing a core set of tests to exercise the main functionality of the VHiSSI FPGA in FIFO mode, and one containing a full set of tests, consisting of the core set plus additional steps, e.g. to test the switching between the nominal and redundant SerDes. Some of the functionality of the Xilinx SerDes used in the VHiSSI FPGA implementation, such as implementation of a redundant channel, does not correspond to the functionality of the SerDes model used in simulation. Therefore, while the full set of tests was used during simulation, the FPGA testing carried out up to this point used the core set. This set of tests exercises the key functionality of VHiSSI in FIFO mode, and the VHiSSI FPGA implementation passed all the tests in this set.

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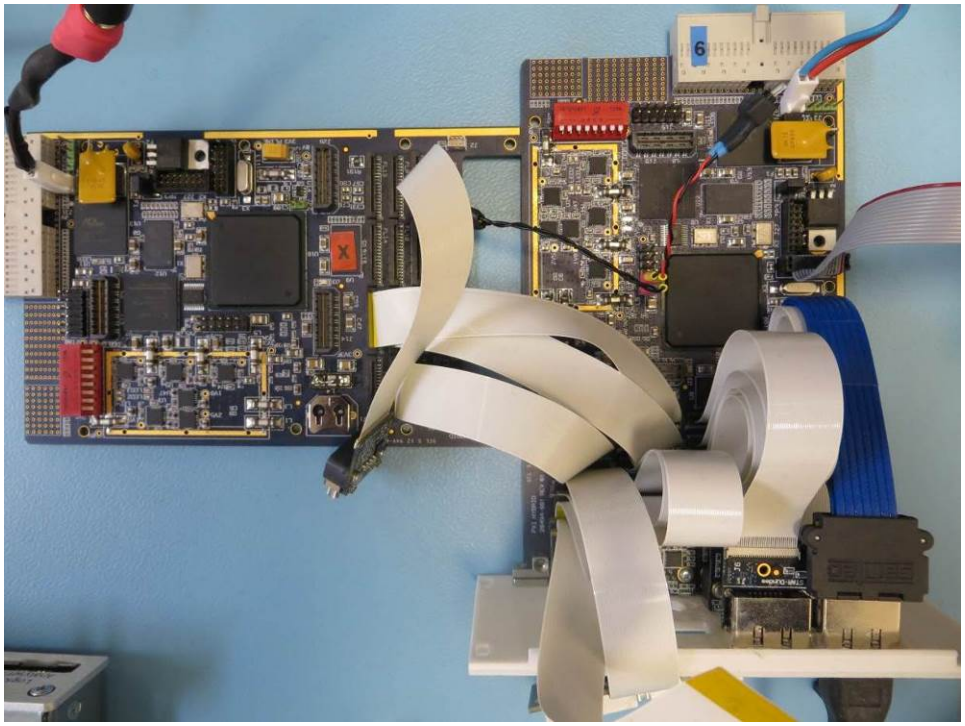

Figure 3-11 Photograph of Parallel Interface Test Setup

The same test architecture used for FIFO mode validation was used for DMT mode validation, with a script file defining the test steps to be executed. This has been tested in simulation, but time did not permit these tests to be carried out on the VHiSSI FPGA implementation.

3.5 WP4 VHiSSI ASIC Research and Design

RAMON carried out the design of the radiation tolerant circuits for the VHiSSI device. RAMON adopted the RadSafe design methodology, which was proved on other products and other process flows, and ported it to IHP 0.13u process. The porting included porting of the schematics and layout to the new process, performing layout verifications, a complete timing characterization and generating the required technology files that enabled the automatic logic and physical synthesis of the RTL based logic design. The key concepts of this methodology are:

- Radiation Hardening is achieved by design - No need for special CMOS process
- Based on standard CMOS technology
- Same technology for all space applications
- Radiation hardening guaranteed by similarity to previously qualified products/test chips
- All IPs fully developed and owned by RAMON. They are completely ITAR free.

The effects mitigated by RadSafe methodology are:

- TID
- SEL
- SEU/SET in flip-flops
- SEU in SRAMs

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The mitigation techniques used are:

- TID – special layout constrains, special SRAM cell
- SEL – special layout constrains
- SEU/SET – special flip-flop circuits, special methodology for clock tree & resetting
- SEU in SRAM – implementing EDAC

3.5.1 Logic Gates

The mitigation of TID effects is done by fix geometry of the transistors, and the parasitic structures. An example of the parasitic devices that are controlled by this methodology is presented in Figure 3-12 which shows an AND gate, with its parasitic devices, controlled in RadSafe technology.

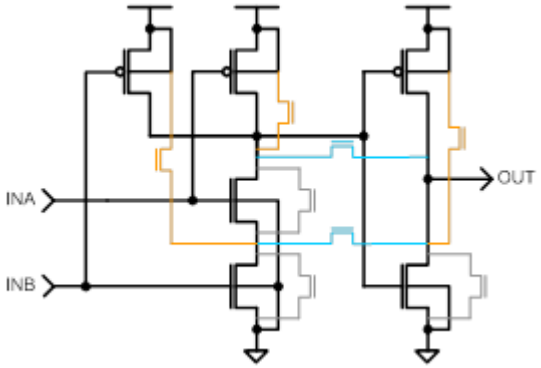

Figure 3-12: Parasitic devices

The mitigation of SEL is done by adequate physical design of the cell libraries. The topology of the PNPN structure, which might latch, is identical in all cells, thus once some of the cells are proven to be immune to SEL, it is true for the rest of the library. The mitigation is achieved by increasing the "holding voltage" of the PNPN devices to be above VDD, thus long term latching is disabled completely.

The mitigation to SEU is achieved by using proprietary circuit, which cannot be upset by flipping of a single node. This is the concept of the flip-flops. The SET effect is mitigated by implementing glitch filter at the input of every flip-flop.

3.5.2 SRAMs

The SRAM cells, which need to be very compact, are also implementing proprietary mitigation technique, which was proven in previous products. It uses 6T circuits, but unlike the conventional circuits, it use 4 PMOS transistors and 2 NMOS transistors. The path transistors, connecting to the bit lines, are implemented by PMOS transistors, which do not leak after TID stress, thus no degradation mechanism exists in this structure. The SEU rate per bit, as measured in previous test chips, was about 10X better than in commercial libraries that is not enough in most space applications, thus EDAC or an alternative fault tolerance technique is needed.

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3.5.3 IO Cells

A combined structure for the IO cells was proposed and implemented in RADIC5. The concept is illustrated in the Figure 3-13. This configurable I/O enables several additional modes of operation, which enhances the performance and flexibility of the VHiSSI significantly. It enables the following features:

- Either 10 single ended SpaceWire ports or 5 differential (LVDS) SpaceWire ports
- TTL2LVDS mode, for additional applications and for easy testing
- LVDS2TTL mode, for additional applications and for easy testing

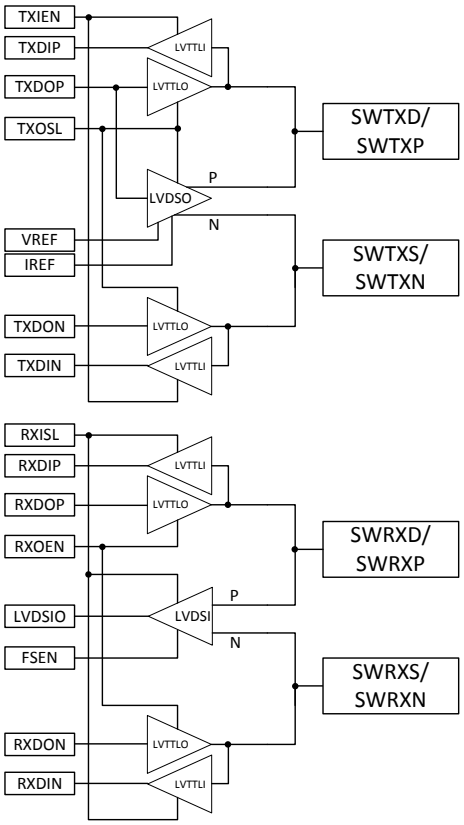

Figure 3-13: Schematics of the configurable TTL/LVDS IO buffers

3.5.4 RADIC5 testing, studying and measuring circuits

This section describes the activities for testing, studying and measuring the circuits including the SerDes on the selected 130nm process using the RADIC5 test chip.

3.5.4.1 Goals of RADIC5 chip

The goals of the RADIC5 test chip were:

- Characterization of the analogue core in bypass mode (eye opening, jitter, BER, etc.)
- Characterization of all I/O cells (VIL/VIH, VOL/VOH, I/O leakage, Vid/Vic of LVDS, etc.)
- I/V characteristics of standard core transistors and their sensitivity to TID stress

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- Speed of ring oscillators, accuracy of the device models and the speed degradation due to TID stress
- Verification of large shift register block, designed with automatic synthesis flow
- Verification of JTAG and boundary scan logic

3.5.4.2 RADIC5 Blocks

The Blocks used in the RADIC5 are listed below:

- SerDes core – analogue core of dual channel SerDes, as provided by ACE-IC
- IO block – the complete ring of I/O pads, with all bonding pads and ESD circuits
- XTOR block – individual RadSafe NMOS and PMOS transistors for I/V characterizations
- RINGS block – 3 ring oscillators/delay lines.
- Logic block – a synthesized logic core, which includes the following functions:
- Switch matrix, to enable operation of the chip in all modes
- JTAG block, which enables boundary scan, and loading the configuration register
- SHFTR block, large block, with 5 shift registers, each one with different flip-flop
- PRBS generator and checker, for characterizing the analogue SerDes

3.5.4.3 RADIC5 Fabrication

The fabrication of the RADIC5 test chip was completed by IHP and packaging was handled by RAMON. The chip layout can be seen in Figure 3-14.

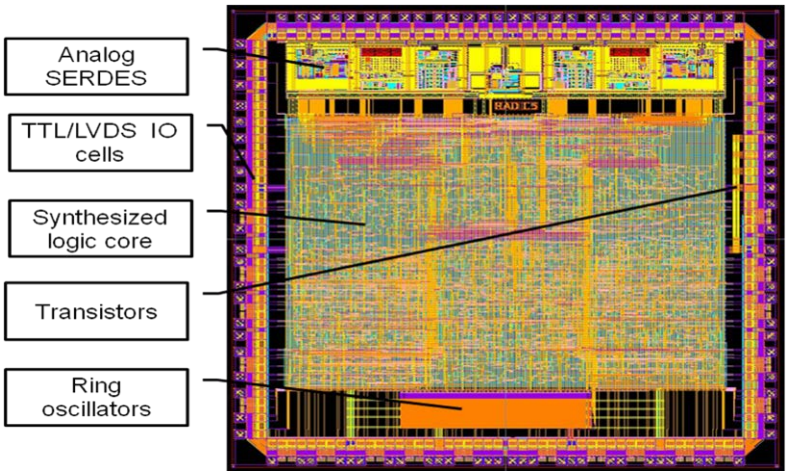

Figure 3-14 RADIC5 Test Chip

3.5.4.4 RADIC5 Testing

The testing of the digital core was completed by IHP and RAMON. The testing of the SerDes by EIT/SCI and ACE-IC was not achieved and STAR took ownership on this task, created a test board and performed, together with ACE-IC, all testing that led to the findings, which were applied to the final delivery of the SerDes.

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The test plan was defined by ACE-IC for the SerDes core and by RAMON for the rest of the chip. The testing of the SerDes core was achieved by testing the SerDes on the board level testing. The test vectors have been generated, but not used.

The testing of the digital parts was done by IHP, based on the test plan and test patterns generated by RAMON. This stage was completed successfully, indicating that all the tested functions are performing correctly.

The list of tests performed is listed in Table 1.

Table 1: RADIC5 testing

#	Test	Test H/W	Owner	Comments	Status
1	Functional & parametric test	VLSI tester	IHP, RAMON	RAMON provided test patterns & test plan. IHP developed the test program	Completed
2	SerDes characterization board	VLSI tester	EIT/SCI, ACE-IC, RAMON	ACE-IC defined test plan. EIT/SCI developing the test H/W & program. RAMON provided test patterns	Completed using STAR board
3	Characterization of transistors	SPA	IHP	Should be done before and after TID stress	Complete
4	TID testing	STAR	ASTRIUM STAR	Logistics & testing should be coordinated with IHP & EIT/SCI	Will be done to VHiSSI

3.5.4.5 Lessons learnt for VHiSSI chip

The following lessons were learnt for the VHiSSI chip during the testing of the RADIC5 test chip:

- All vias should be duplicated.
- Should consider the use of the multi-IO buffers with ODT to enable termination of input signals.
- Filler cells should not have any sensitivity to yield. Capacitance is less important.
- Assembly of the VHiSSI devices should come from several wafers, and defect density of the yield monitors should be considered when selecting the wafers to be assembled.
- The EVCD files should include all the pins, including the analogue pins and IREF/VREF pins (even if it defined as high impedance).
- Test Rule Checker (TRC) should be run as "tapeout procedure" to the test patterns.
- In LVDS+TTL buffers, verify that pull-up transistor is disconnected when LVDS is active.
- Timing of all inputs should be aligned, as much as possible, to simplify the patterns. In many cases, the NRZ signals can change at FE of CLK.

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3.5.5 Integration and verification of the VHiSSI experimental device

In this section the Integration and verification of the VHiSSI experimental device, done by RAMON are described. The VHiSSI top level architecture is shown in Figure 3-15.

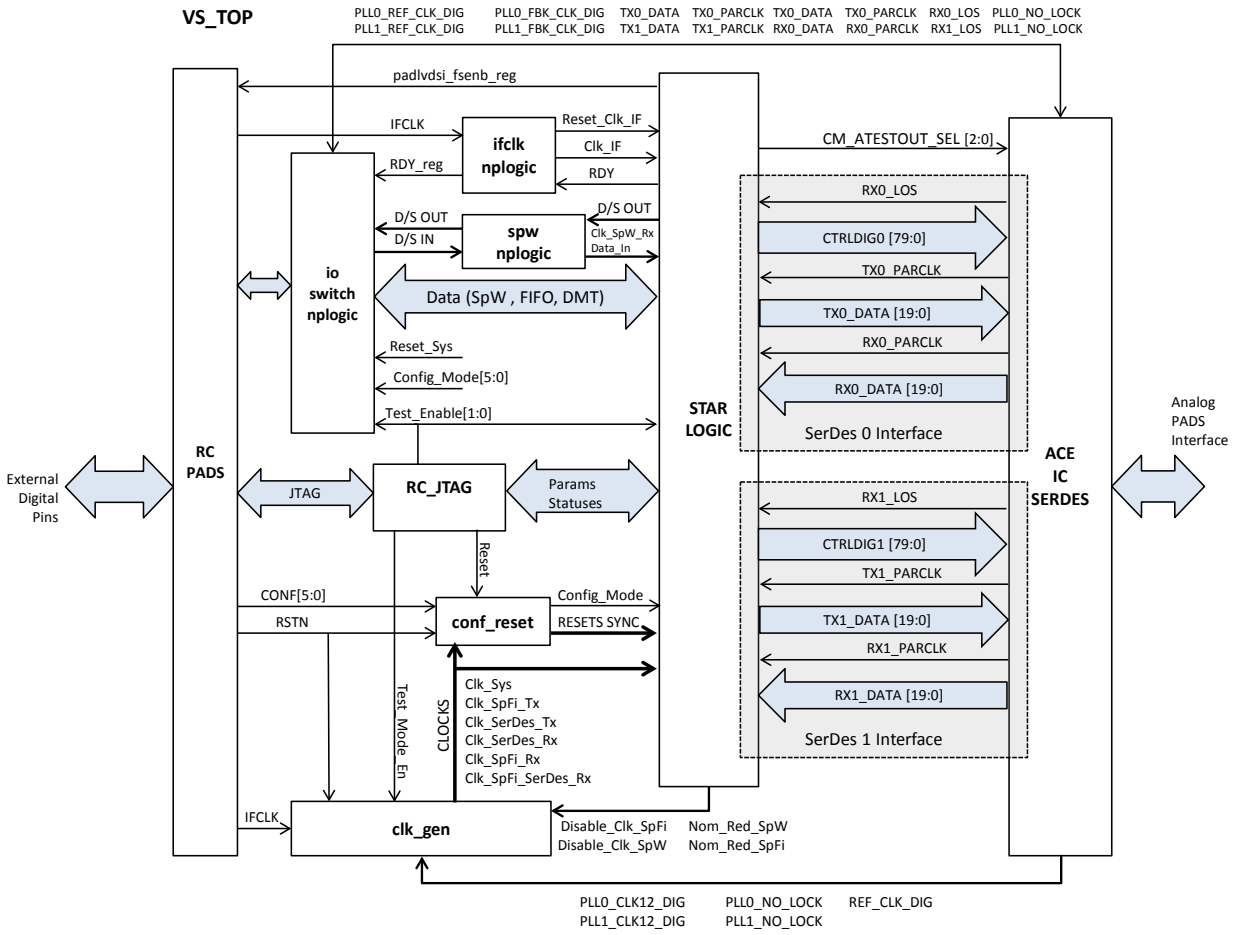

Figure 3-15: VHiSSI Top Level

Top level contains the following main modules:

- **RC_PADS**: IO pads provided by RAMON including LVTTL and LVDS drivers.
- **RC_JTAG**: JTAG controller designed by RAMON.
- **STAR_LOGIC**: Designed by STAR. Provides the main functionality of VHiSSI including the SpaceWire router and the SpaceFibre codec. It also includes the BIST controller designed by RAMON.
- **ACE_IC_SerDes**: Designed by ACE-IC. Provides an analogue core that implements a SerDes.

In addition, there are some small modules in the Top Level module:

- **io_switch_nplogic**: Connects the various digital interfaces within the VHiSSI chip to the digital IO pins, depending on the strapping pins and the *Test_Enable* signal. Also contains some registers that shall be located close to the pads.
- **conf_reset**: Creates the synchronous resets for *Clk_Sys* and *Clk_IF* domains and latches the values of the CNF[5:0] pins when RSTN pin is low.

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- **ifclk_nplogic**: Contains the logic related with the *Clk_IF* domain that needs to be placed as close as possible to the pads (Near Pad Logic). Generates the *Clk_IF* signal. Registers the *RDY* signal close to the output pad.
- **clk_gen**: Generates all clocks except the *Clk_IF*.
- **spw_nplogic**: Defines the logic related with the *Clk_Spw_Tx* domain that needs to be placed as close as possible to the pads (Near Pad Logic). Recovers the *Clk_Spw_Rx* clocks immediately after Data and Strobe signal enter the chip to minimise the skew between them, and also recovers the SpW input bit stream with this clock.

3.6 WP5 VHiSSI PHY Layer Research and Design

The SerDes is a key element of the VHiSSI chip which converts parallel data to high-speed serial data and vice versa. A block diagram of the final SerDes is illustrated in Figure 3-16.

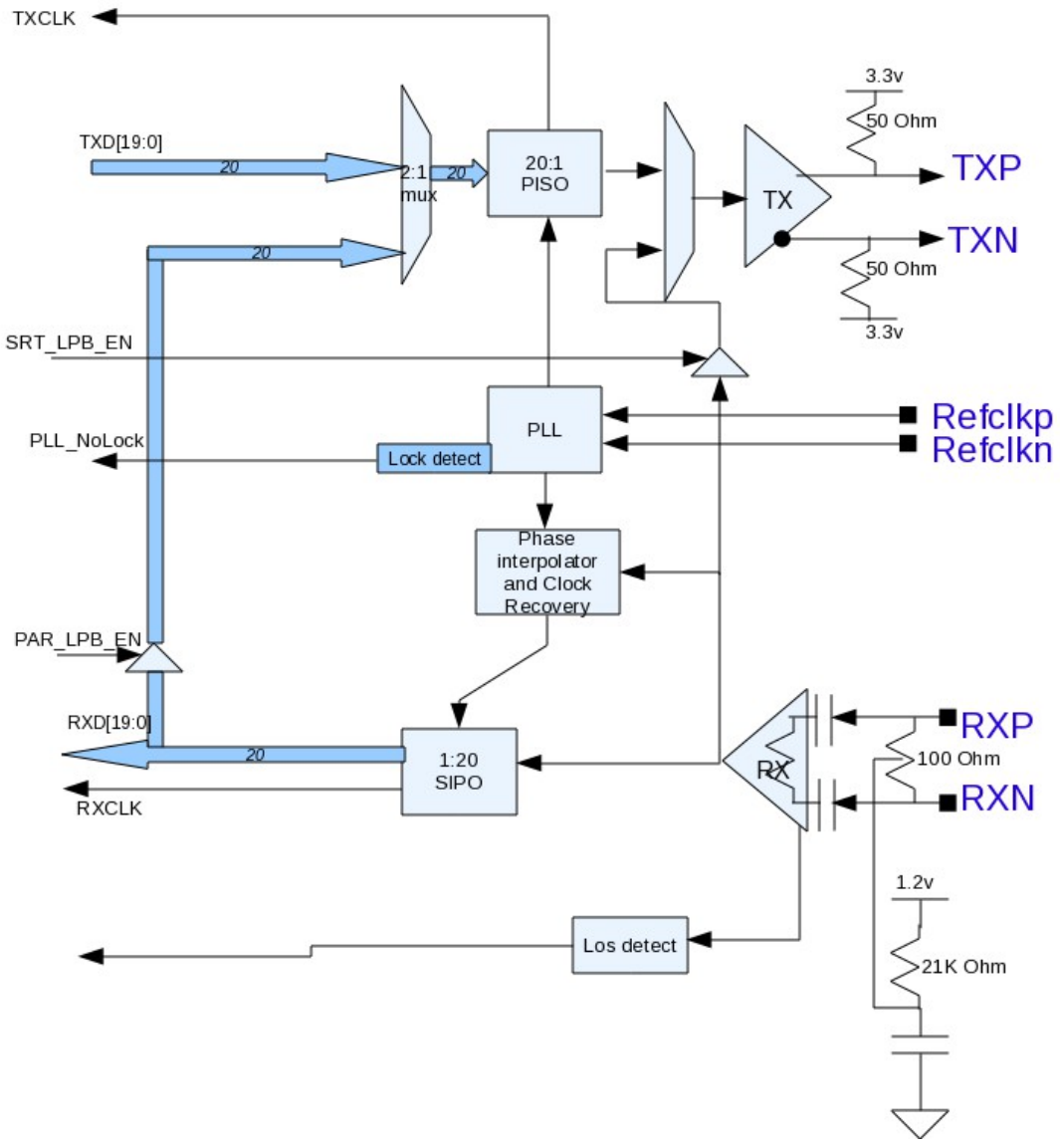

Figure 3-16 - SerDes Block Diagram

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The transmit data (TXD[15:0] is passed via a 2:1 multiplexer into the parallel in to serial out (PISO) converter which converts the 20-bit encoded data into a serial bit stream. The serial bit stream is then passed to the transmit driver providing the differential CML transmit signals (TXP and TXN). A transmit clock operating at 1/20 of the required data rate is proved by a PLL in the SerDes to be used for loading of parallel transmit data into the SerDes.

The serial received CML data (RXP and RXN) is received by the CML receiver and passed via a 2:1 multiplexer to a serial in parallel out (SIPO) converter, to the clock recovery circuit and to a loss of signal detector (LOS). The SIPO converter takes the serial data and a recovered clock signal provided by the clock recovery circuit, samples the received signal, takes 20-bits of the serial data and converts them to 20-bit parallel data. A receive clock at 1/20 of the received data rate is provided for transferring the decoded parallel data out to user logic.

The PLL is provided with a reference clock from which it generates the transmit clock, and a reference clock for the Phase Interpolator and Clock Recovery circuit. The Phase Interpolator and Clock Recovery circuit locks to the phase of the received signal to provide a receive sampling clock.

The loss of signal detector (LOS) detects when there is no signal present at the input of the receiver.

Two loopbacks are provided: a serial loopback that connects the receive serial data signal to the input of the transmitter and a parallel loopback that connects the received parallel data output to the transmit parallel data input. These loopback circuits are controlled by signals STR_LPB_EN and PAR_LPB_EN respectively.

The PHY circuits were layout by ACE-IC, RAMON provided the STD cells and I/O cells and customized the ESD to meet low capacitance requirement of the SerDes.

The final SerDes layout is shown in Figure 3-17.

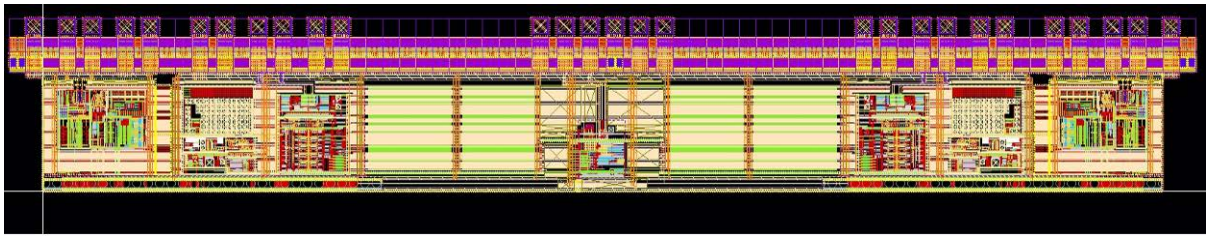

Figure 3-17: SerDes layout

3.7 WP6 VHiSSI ASIC Experimental Implementation

WP6 focused on implementation, packaging and initial tests of the final VHiSSI chip. The VHiSSI chip design was exported to the IHP fab on April 2014 and it was included in a multi project wafer (MPW) run. Chips were produced in the period April - July 2014 and selected wafers passed the acceptance tests defined by IHP- internal rules. Diced chips were sent to the subcontractor MAF for packaging. After receiving the 90 packaged devices, the initial test campaign started in the second half of August.

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3.7.1 Chip Fabrication Process

The VHiSSI chip was submitted to the MPW run for 130 nm technology. This technology was still at the research stage and was not commercially qualified. Some basic information about the clean room of IHP is provided in the following Figure 3-18. Also the view to the IHP clean room during fabrication process is given in Figure 3-19.

CLEANROOM SIZE	~ 1000 m² Class 1
TECHNOLOGY	RF SiGe:C BiCMOS
WAFER SIZE	200 mm
CAPACITY	100 Wafer Starts / Week
TOOL SET CAPABILITY	0.25µm / 0.13 µm
MODE OF OPERATION	24h, 7 Days / Week
SiGe:C BiCMOS Cycle Time	≥1.7 Days / Mask level

Figure 3-18 Summary of IHP Clean Room Features

Figure 3-19 View to the IHP Clean Room

The VHiSSI chip was submitted to the multi-project wafer (MPW) run. That means that several chips share the mask costs and that they are fabricated in parallel.

3.7.2 VHiSSI Packaging

The package selected for VHiSSI is a 14x20mm 100L QFP. It provides sufficient IOs, and the electrical performance of the traces is marginally acceptable for the required data rate of the SerDes.

The bonding diagram of VHiSSI is the presented in Figure 3-20. The lead frame was replaced relative to the one used in RADIC5 to the selected one in order to have a larger die pad, required for larger die size, and shorter lead traces, which have less inductance. The increase of the die size and shortening the bond wires provides an additional advantage, thus the total reduction of the inductance

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of the lease is 1-2nHy, or 10-20%. This improvement in package performance will be translated to some improvement in signal integrity of the high speed signals.

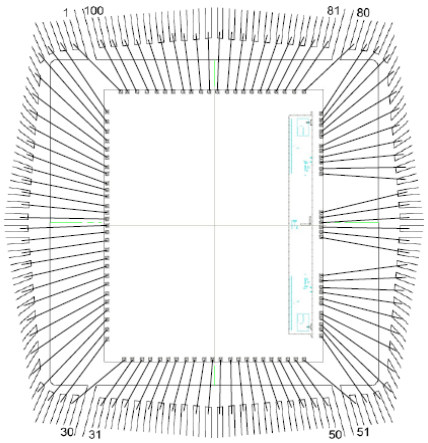

Figure 3-20 Bonding diagram of VHiSSI chip (die pad is 9.5x9.5mm)

The device is packaged in plastic QFP package for the purpose of this project. It is possible to convert this package to an equivalent hermetic ceramic package, with similar dimensions and similar electrical performance, which will allow this product to be modified to space qualified package. This is an option for future productisation of this product and qualifying it for space.

3.7.3 VHiSSI Initial Test

After receiving the packaged chips, the initial test campaign was started in IHP with staff support from STAR and Synergie-CAD. 90 packaged devices were received and it was decided to perform the tests on 65 devices while 25 were kept as a backup. The following sets of tests were made using a VLSI tester.

- Continuity test
- Static IDD
- Reset test
- IDDQ Test
- IO Tests – lvds2lvttl and lvttl2lvds
- Functional – FIFO tests (only limited tests available)
- Functional – SPW tests (only limited tests available)
- Functional – memory BIST tests (due to an error in the design only one memory block had BIST connected).
- SerDes – DC Tests
    - SerDes – Power down
    - SerDes – Power up

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- SerDes – Power down/ Rx on
- SerDes – Vout-Bref
- SerDes – Vout-Power up

From the tested 65 chips, the pre-selection process had already discarded 11 chips based on the continuity tests (determined by packaging). The other main tests such as static Idd, Iddq, functional, SerDes tests discarded an additional 2-5 chips, with the tendency that the same chips usually failed on multiple tests.

Although the current tests have shown very promising results and low dispersion of the measured current values among the different chips, the open question regarding the yield has been opened with the BIST test which revealed 11 erroneous chips, with only testing the single block of memory. The next system level test will determine whether the memory yield could be an issue for system testing of the SerDes or not.

As a final result, of the initial testing 36 chips (out of 54 passing continuity) have been selected as suitable for use in the next phase of system testing, SerDes characterization and radiation testing. Test vectors to test most of the chip functionality were not ready in time for the tests on the VLSI tester so these tests were carried out in WP7 using dedicated test boards.

3.8 WP 7 ASIC Experimentation and Testing

The VHiSSI chips that passed the testing on the VLSI tested at IHP were subject to further testing and experimentation by STAR-Dundee, UNIVDUN and ACE-IC. To support this testing several test boards were designed by STAR-Dundee.

3.8.1 Test Boards

This section describes the circuit boards necessary for the experimentation on the SpaceFibre-HSSI chip. Four test boards were required to test the different VHiSSI operational modes and to support radiation testing:

- VHiSSI SpaceWire LVDS Test Board
- VHiSSI SpaceWire LVTTL Test Board
- VHiSSI Parallel Interface Test Board
- VHiSSI Radiation Test Board

The VHiSSI SpaceWire LVDS Test Board is used to test the SpaceWire to SpaceFibre bridge mode of the VHiSSI chip using the inbuilt LVDS drivers for SpaceWire giving 5 LVDS SpaceWire ports and one LVTTL port. This board was also designed to support the single event effect (SEE) radiation testing. A block diagram and photograph of the SpaceWire LVDS board is shown in Figure 3-21.

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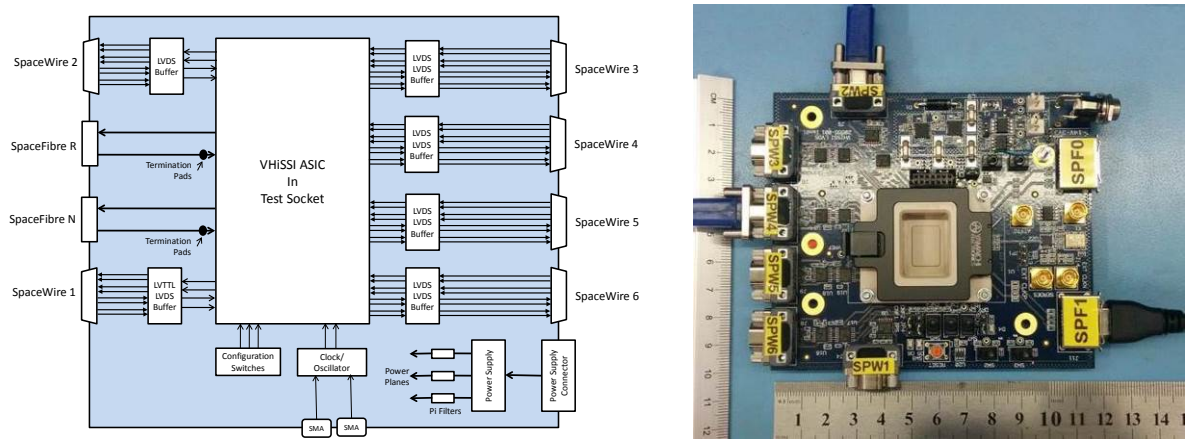

Figure 3-21 VHiSSI SpaceWire LVDS Test Board

The VHiSSI SpaceWire LVTTL Test Board is used to test the SpaceWire to SpaceFibre bridge mode of the VHiSSI chip using the inbuilt LVTTL drivers for SpaceWire giving 11 SpaceWire LVTTL ports. A block diagram and photograph of the SpaceWire LVTTL board is shown in Figure 3-22.

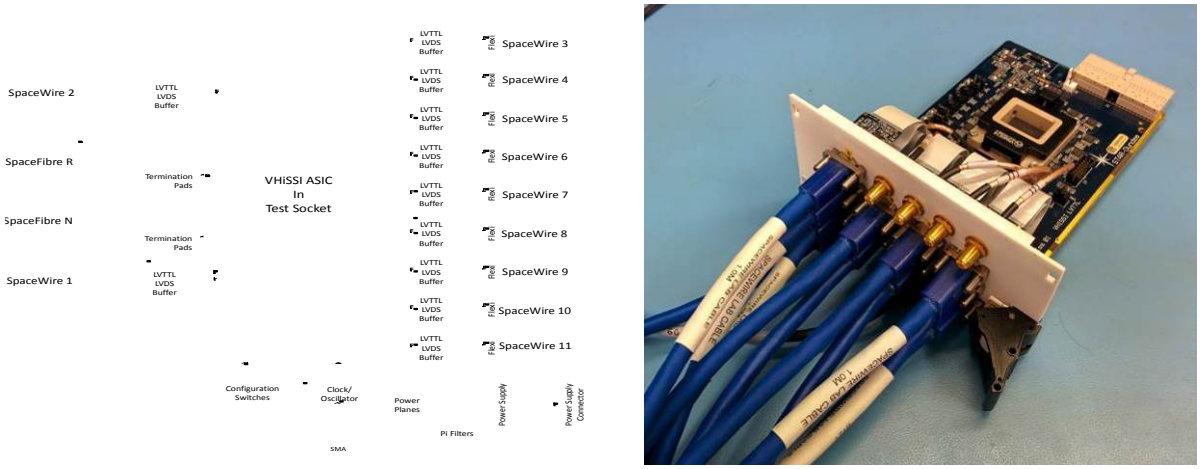

Figure 3-22 VHiSSI SpaceWire LVTTL Test Board

The VHiSSI Parallel Interface Test Board is used to test the VHiSSI chip operating with the parallel interface to the VHiSSI chip including the FIFO, Memory and DMA interfaces. A block diagram and photograph of the Parallel Interface board is shown in Figure 3-23.

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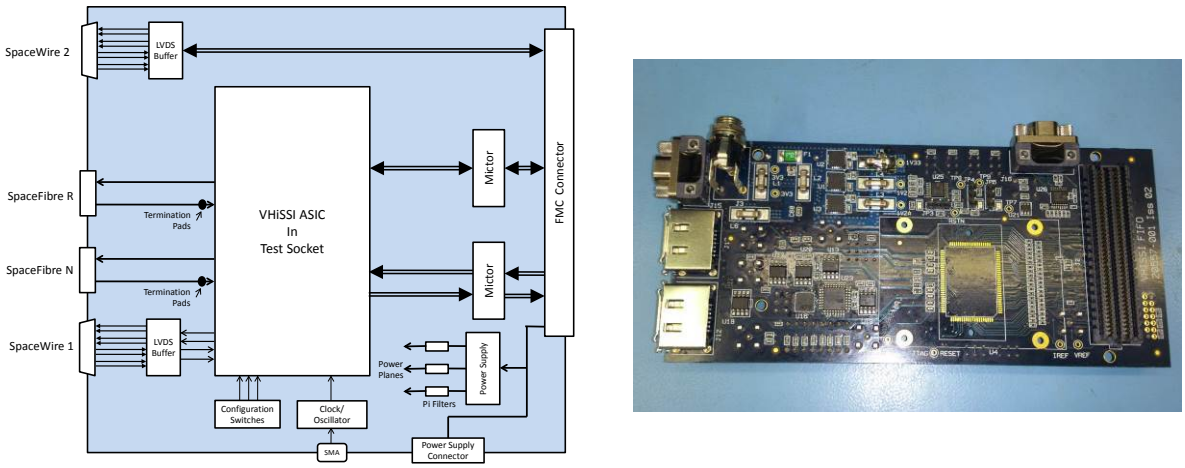

Figure 3-23 VHiSSI Parallel Interface Test Board

3.8.2 SerDes Testing

The SerDes characterisation test setup is shown in Figure 3-24.

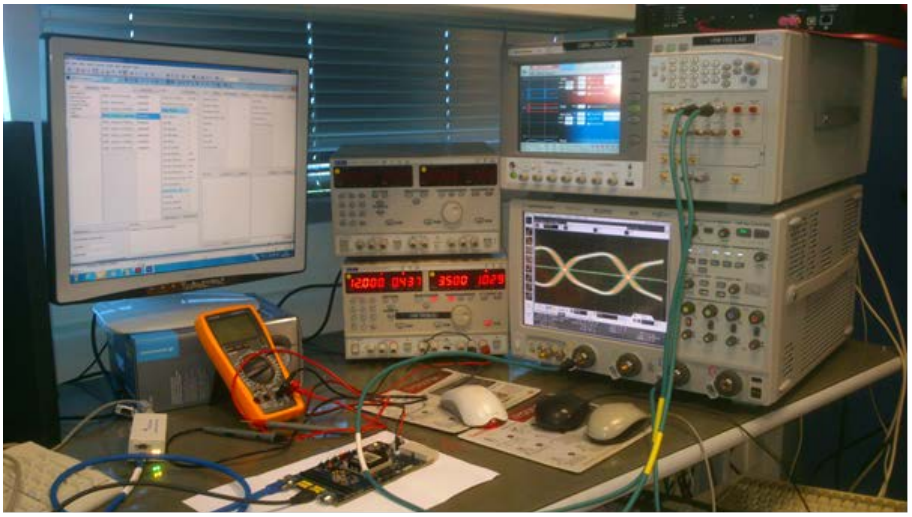

Figure 3-24 SerDes Characterisation Test Setup

A SpaceWire-USB Brick is connected to one of the VHiSSI SpaceWire LVTTL board's SpaceWire connectors and to the host PC through its USB interface. Software provided by STAR-Dundee is used to control the system and change registers values in the VHiSSI chip. A JBERT Bit Error Rate Tester is connected to the receive (RX) side's high speed serial SpaceFibre interface and is used as serial data source generator to create clock patterns and PRBS patterns. The oscilloscope or JBERT input is connected to the transmit (TX) side to measure serial output signal transmitted from the chip. When a RX to TX parallel loopback is closed, the data received by the VHiSSI chip should be transmitted back out of the VHiSSI chip.

The overall performance of the SerDes was within the expected design values. The design improvements made to the SerDes in the VHiSSI chip following the results of the RADIC 5 testing

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were all found to operate as intended, significantly improving the SerDes operation. The eye pattern of the SerDes is shown in Figure 3-25.

Figure 3-25 TXPLL Eye Diagram - Optimal Settings

3.8.3 Functional Testing

Functional testing of the VHiSSI chip was carried out by STAR-Dundee and UNIVDUN.

3.8.3.1 SpaceWire LVDS Mode

In the VHiSSI SpaceWire LVDS mode of operation up to five SpaceWire interfaces are each provided with LVDS drivers/receivers. The following set of tests were run on the VHiSSI chip to test the SpaceWire LVDS mode. In all 171 separate tests were run to test the SpaceWire LVDS mode.

1. **Basic Register Tests:** Check that all VHiSSI registers are accessible and have the expected reset values, except for the status register of the SpaceWire port being used to read the VHiSSI registers.
2. **Router Tests:** Check VHiSSI links 1, 2 and 3 at different speeds, and the internal router operation.
3. **SpaceFibre Loopback Tests:** Check that SpaceFibre parallel loopback works and all virtual channels (VCs) connected to SpaceWire links work correctly.
4. **SpaceFibre SerDes Tests:** Checks that nominal and redundant SerDes and its interface with SpaceFibre logic works.
5. **SpaceWire Packet Stress Tests:** Send SpaceWire packets of multiple sizes, testing different corner cases for the most interesting packet sizes.

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Figure 3-26 shows the VHiSSI SpaceWire LVDS test board (on the right hand side of the figure) attached to the test equipment. This setup allowed all SpaceWire interfaces on the SpaceWire LVDS test board to be tested extensively using automated software tests.

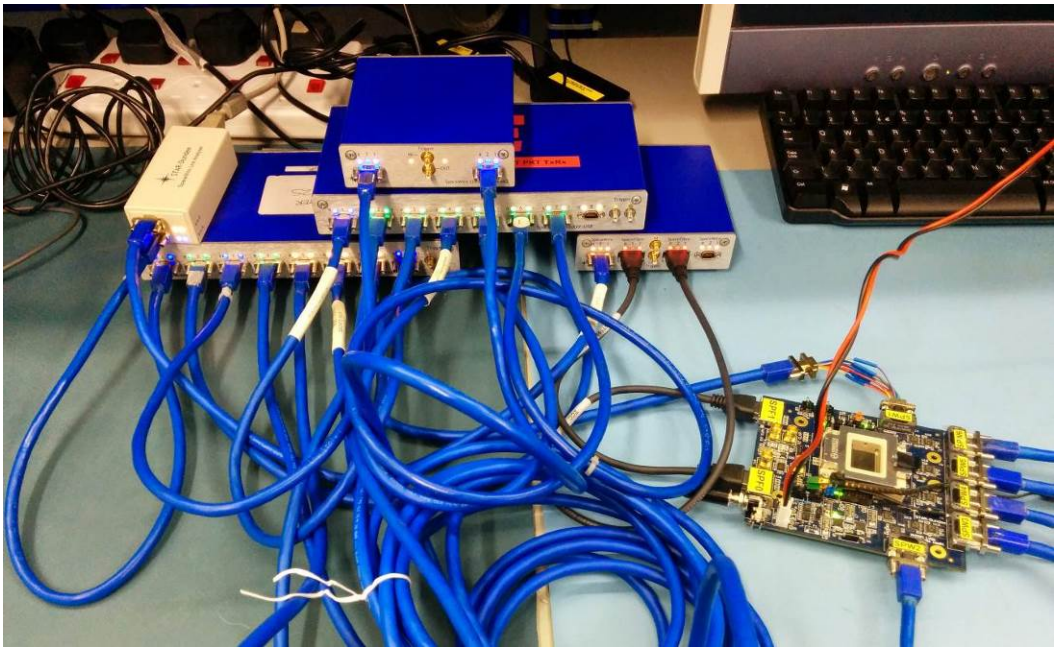

Figure 3-26 Test Setup for the VHiSSI SpaceWire LVDS Testing

3.8.3.2 SpaceWire LVTTL Mode

In the VHiSSI SpaceWire LVTTL mode up to eleven SpaceWire interfaces are provided each with LVTTL drivers/receivers. On the VHiSSI SpaceWire LVTTL Test Board all eleven LVTTL SpaceWire ports are implemented.

The SpaceWire LVTTL mode tests consist of a single test group comprising 126 separate tests:

SpaceWire Packet Stress Tests: Send SpaceWire packets of multiple sizes, testing different corner cases for the most interesting packet sizes.

3.8.3.3 Parallel Interface Mode

The Parallel Interface mode of operation of the VHiSSI chip was tested in a different way to the SpaceWire Bridge mode tests. The Parallel Interface tests were designed to execute the same set of tests as the VHDL test bench to confirm that the hardware operation was the same as the simulated operation. As described in section 3.4.4 a dedicated test board was designed using a commercial Xilinx FPGA board. The VHiSSI Parallel Interface board was plugged into this test board via an FMC connector, which carried the parallel interface signals of the VHiSSI chip to the Xilinx FPGA. The Xilinx FPGA was programmed to exercise each of the parallel modes of operation of the VHiSSI chip and to record the results for analysis. Initially the tests were run at 10 MHz to confirm operation of the test logic. The tests were then run at full speed to confirm correct operation of the VHiSSI chip.

On the VHiSSI parallel mode test board a pair of Mictor connectors were provided to enable connection to a logic analyser. This was very useful in debugging the test application on the Xilinx

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FPGA. A screenshot from a logic analyser showing the FIFO mode of operation of the VHiSSI chip is shown in Figure 3-27.

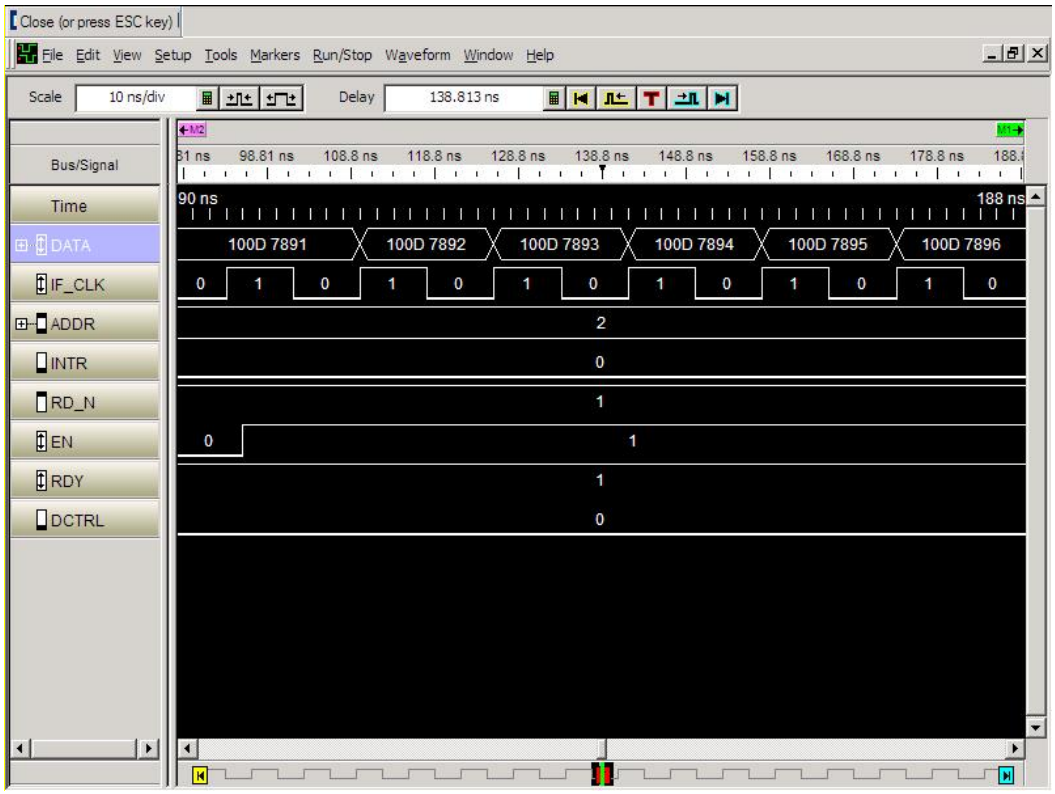

Figure 3-27 Screenshot of Parallel Interface Signals on Logic Analyser – FIFO Mode

3.8.3.4 Function Testing results

Extensive functional testing has been carried out on the experimental VHiSSI chip, covering all the principal modes of operation of the device:

- SpaceWire LVDS Bridge Mode
- SpaceWire LVTTL Bridge Mode
- Parallel Interface FIFO Mode
- Parallel Interface Memory Access Mode
- Parallel Interface DMA Mode

Figure 3-28 shows the combined results of the functional validation activity. Thirty-nine VHiSSI chips were tested. The test results from each chip are summarised in a column. For each test carried out, a pass is indicated by a green block. A red block indicates a test failure, and for each failure a separate row indicates the reason for the failure, with another red block mapping the fault to the failing chip. A black border is used to indicate the chips which passed all tests.

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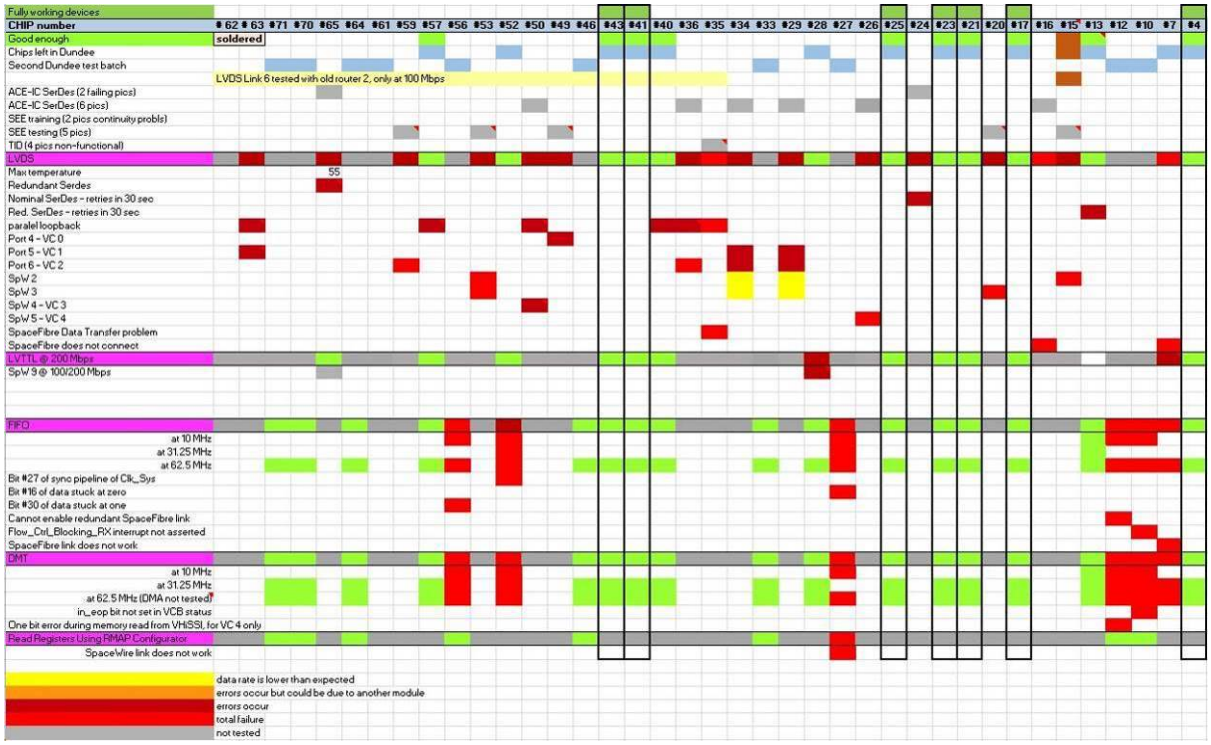

Figure 3-28 Functional Validation Results

The final selection shows 7 fully working devices out of the 66 originally (~11% fully functional devices). Out of the first batch of 29 chips that passed the tests carried out on the VLSI tester, 27 were fully tested with a total of 7 passing all functional tests. Some of the chips that failed to pass all the tests were fully operational in some modes of operation. The failures were generally different for each chip tested.

These results indicate that the design is functional and that the VHiSSI chip fulfils its design goals. It is rather disappointing, however, that the number of fully functional devices was low. It is possible that some of the problems detected may be due to timing issues with the layout of the device. Further experimentation is required to help determine this is the case. It is planned to carry out tests on faulty parts at different temperatures and with different supply voltages to see if the failure disappear which would indicate a possible timing related issue.

A device that fails because of a fault on one SpaceWire interface, for example, will still be usable for any subsequent test or demonstration that does not use that SpaceWire interface. A fault with the parallel loopback does not affect the operation of the VHiSSI chip as this is a test circuit.

The lack of fully functional devices led to a problem when deciding which chips should be used for parallel interface, TID radiation, SEE radiation and SerDes characterisation tests which, owing to time constraints, had to all be run in parallel. It was decided to keep all of the best chips for parallel interface testing

Parallel Interface Testing: The fully functional VHiSSI chips were reserved for the Parallel Interface functional testing.

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TID Radiation Testing: For the TID testing the main pre and post irradiation tests were on measurements of the characteristics of device, e.g. static current. Four chips were selected from those that had failed tests to save the more functional ports for other types of test.

SEE Radiation Testing: Five devices were selected where there were problems with a single SpaceWire interface or single virtual channel in the SpaceFibre interface. It was possible to operate the VHiSSI chip, configuring it and sending and receiving data using SpaceWire interface 1. This would allow the registers of the chip to be read and monitored for changes during irradiation using SpaceWire interface 1. Test software was written to support the monitoring of all the VHiSSI chip registers.

SerDes Characterisation: Five chips were selected where there were problems with a single SpaceWire interface or one or two virtual channel in the SpaceFibre interface. It was thought that these problems, being outside the SerDes part of the circuitry, would not affect the results of the SerDes characterisation. Another chip was selected where the SpaceFibre interface would not connect. This device was an example of a possible faulty SerDes. In addition a further two chips were provided for the SerDes testing: one in which the redundant SerDes had CRC and other errors and the other in which the nominal SerDes failed after about 30 s.

3.8.4 Performance Assessment

Performance assessment was carried out at the same time as the functional testing and characterisation was being carried out.

3.8.4.1 Performance Test Set Up

Figure 3-29 shows the test setup used during assessment of the performance of the VHiSSI chip operating at different SerDes speeds.

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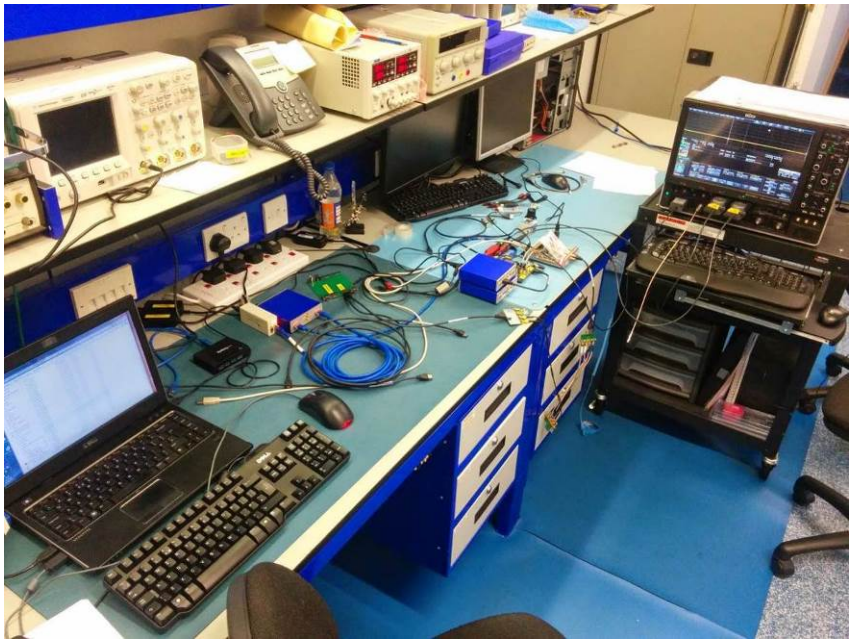

Figure 3-29 Performance Assessment of the VHiSSI Chip

To monitor the eye diagram of the VHiSSI chip a LeCroy Digital Oscilloscope with 16 GHz bandwidth and sampling rate of 40 Gsamples/s was used. 6 GHz bandwidth differential probes were used to monitor the transmit and receive signals from the VHiSSI chip.

The following performance related tests were carried out on the VHiSSI device:

- **SerDes:** The SerDes including the clock data recovery was tested at nominal 2.5 Gbits/s and also at 3.125 and 3.5 Gbits/s. In each case the link was checked to ensure that there were no errors and the eye pattern was recorded to gauge its suitability.
- **SpaceWire LVDS:** The SpaceWire LVDS interfaces were tested at 10, 50,100 and 200 Mbits/s during the functional tests T2.5 to T2.45. All functional devices achieved the goal of 200 Mbits/s link signalling speed.
- **SpaceWire LVTTL:** The SpaceWire LVTTL interfaces 2 to 11 were all operated at 200 Mbits/s during the functional SpaceWire LVTTL tests (Tested at the top speed of 200 Mbits/s (T2.172 to T2.298). SpaceWire LVTTL interface 1 was tested at 10 Mbps as it is also used for communication with the PC. However, this interface is available in all functional modes and in LVDS mode it was tested at 100 Mbps.
- **Parallel Interface:** The Parallel Interface was tested in FIFO and Memory modes tested with an interface clock (IFCLK) of 10, 31.25 and 62.5 MHz and in DMA mode with an interface clock of 10 and 31.25 MHz. The speed of the DMA mode interface was limited by the speed of the external memory in the FPGA.

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3.8.4.2 Performance Test Results

The performance of the interfaces of the VHiSSI chip are summarised in Table 3-2. All the interfaces of the VHiSSI chip performed at the speed they were designed to operate at. The SpaceFibre interface was able to operate at 3.125 Gbits/s but the eye pattern was not acceptable at this speed.

Table 3-2 VHiSSI Interface Performance

Interface	Target Performance	Achieved Performance
SpaceWire LVDS	200 Mbits/s	200 Mbits/s
SpaceWire LVTTL	200 Mbits/s	200 Mbits/s
Parallel Interface: FIFO	62.5 MHz	62.5 MHz
Parallel Interface: Memory	62.5 MHz	62.5 MHz
Parallel Interface: DMA	Depends on speed of external memory	31.25 MHz
SerDes	2.5 Gbits/s	2.5 Gbits/s

The eye pattern of the SpaceFibre signal from the VHiSSI chip before SerDes optimisation is shown in Figure 3-30.

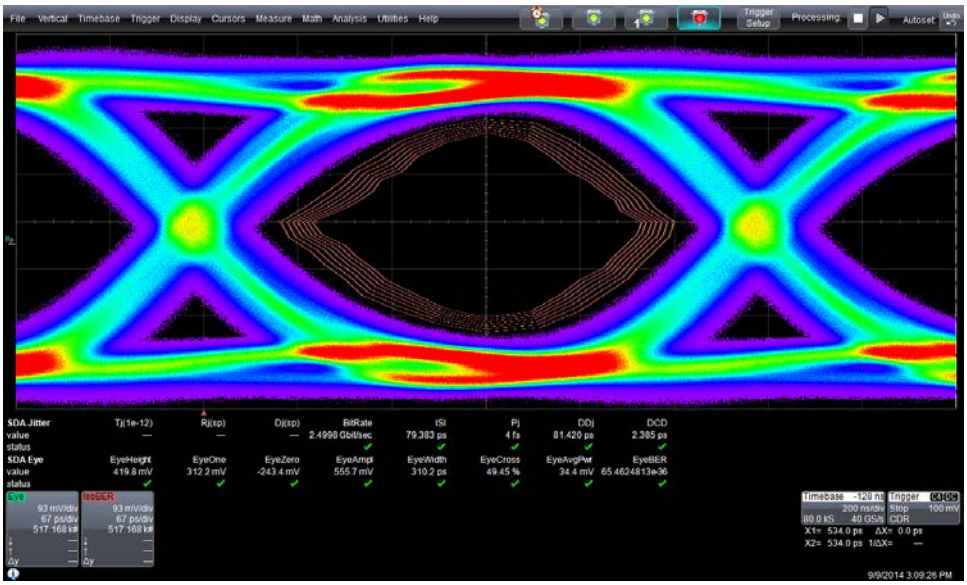

Figure 3-30 VHiSSI SpaceFibre Receive Eye Pattern at 2.5 Gbits/s

3.8.5 System Level Experimentation

3.8.5.1 Experiments

Experiments were made on the VHiSSI chip to confirm the operation of the QoS (deterministic scheduling, priority and bandwidth reservation) and to check that remote access to VHiSSI control

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and status registers was possible over SpaceFibre. In addition two important application driven modes of operation for the VHiSSI chip were explored: providing a SpaceFibre interface to a high data-rate instrument using the FIFO mode of operation and SpaceWire to SpaceFibre bridging. The results obtained illustrate the diverse applications of the powerful VHiSSI SpaceFibre high speed serial interface chip. One of the experiments run is described in more detail in the following subsection.

3.8.5.2 SpaceWire to SpaceFibre Bridge Operation

SpaceWire to SpaceFibre bridging is an important mode of operation for the VHiSSI chip. In this experiment 10 SpaceWire links all operating at 200 Mbits/s in both directions were multiplexed over a single SpaceFibre interface. The test set up used for this test is illustrated in Figure 3-31.

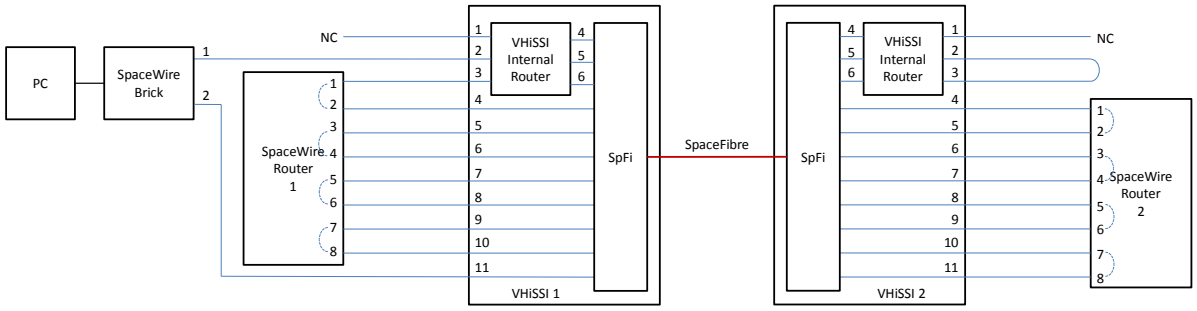

Figure 3-31 SpaceWire to SpaceFibre Bridge Experimental Setup

Two VHiSSI chips are connected together via a 2.2 m SpaceFibre cable. SpaceWire port 1 is not used on either VHiSSI chip. VHiSSI chip 1 is connected to ports 1 and 2 of a SpaceWire Brick via ports 2 and 11 respectively. The remaining ports of the VHiSSI chip 1 (ports 3 to 10) are connected to ports 1 to 8 of a SpaceWire router. The second VHiSSI chip has ports 2 and 3 connected together and the remaining ports (ports 4 to 11) are connected to ports 1 to 8 of a SpaceWire router. A host PC is used to start all the links of each the two routers and to start the SpaceFibre link. SpaceWire packets are then generated and sent through port 1 of the SpaceWire Brick to port 2 of the internal router in VHiSSI 1, though the SpaceFibre link, to VHiSSI 2 internal router.

A SpaceWire path address of 1 5 2 6 3 2 2 4 4 6 6 8 8 2 7 7 5 5 3 3 1 1 6 3 5 2 will route the packet through all the SpaceWire links and back again so that there are 10 SpaceWire links at each end of the SpaceFibre link running at 200 Mbits/s (~150 Mbits/s data rate) in each direction. The maximum data rate at which packets could be generated on the test PC being used was 147 Mbit/s giving an aggregate data rate through the SpaceFibre link of 1.47 Gbits/s in each direction (approximately 1.8 Gbits/s after 8B10B encoding).

A photograph of this set up demonstrating SpaceWire to SpaceFibre bridging is shown in Figure 3-32.

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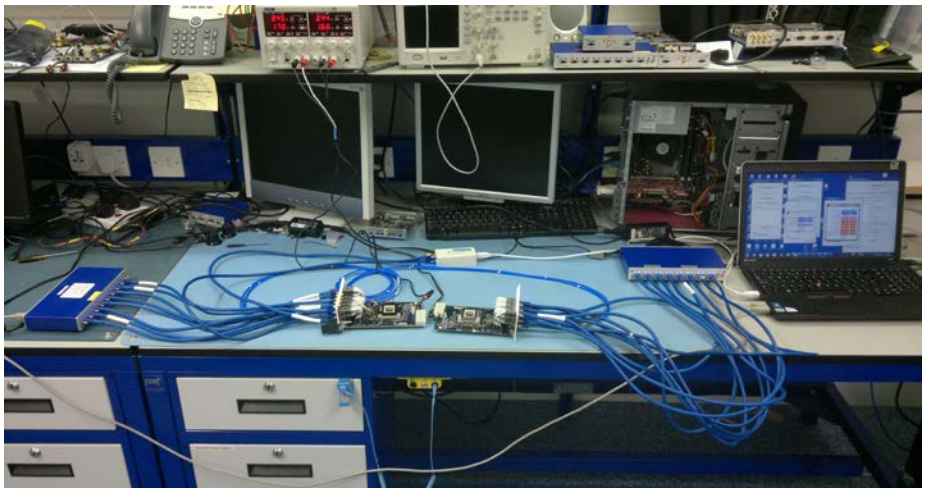

Figure 3-32 Photographs of SpaceWire to SpaceFibre Bridge Experimental Setup

The data rate achieved over in each direction of each of the ten SpaceWire cables is shown in Figure 3-33.

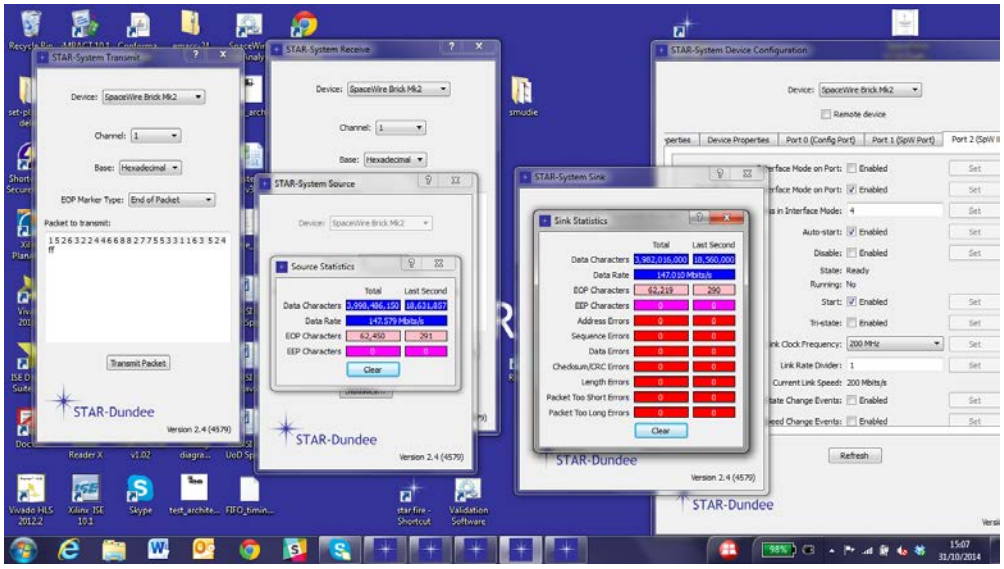

Figure 3-33 Screen Shot of Test Software Running the SpaceWire to SpaceFibre Bridge Experiment

The data rates of the source and the sink are 147 Mbits/s resulting in all ten SpaceWire links transmitting and receiving at 147 Mbits/s giving the total data rate over the SpaceFibre link as 1.47 Gbits/s in each direction. The operation of the SpaceWire to SpaceFibre Bridge was clearly demonstrated.

3.8.6 Total Ionising Dose (TID) Radiation

The TID radiation tests were carried out by Airbus DS, IHP and STAR-Dundee.

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3.8.6.1 Description of the Radiation Source

For the TID testing a Gammacell ^{60}Co was used with a rate of about 10 Gy/min (Figure 3-34). The test board is located within a closed unit irradiation chamber of 20.6 cm height and 15.2 cm diameter.

The right hand photograph in Figure 3-34 shows an example of a test board which is located in the irradiation chamber. During irradiation the chamber will be lifted down inside the radiation field.

In the case of the VHiSSI chip the test board is irradiated. All other equipment like power supply is outside the chamber and is not affected by any radiation field.

Figure 3-34 ^{60}Co Source for TID testing (left) and Cylindrical Chamber with an Example of a Test Board (right)

3.8.6.2 List of Tests Performed and Test Concept

The Radiation Total Ionising Dose (TID) test campaign for the VHiSSi chip was planned and executed. The total dose with which the chips were radiated was 300 kRads. The TID test approach used was similar to the one developed for previous RADIC5 test chip.

Functional, performance and power tests on digital and analogue VLSI structures, were performed using Advantest 93k SoC test platform. For analogue structures, i.e. the SerDes, only DC tests were performed.

The general test campaign was the following:

1) Pre-radiation tests including execution of the full TID test suite

2) Irradiation 300krad

3) Post-radiation tests (delay of approx. 6 Hours) - including execution of the full TID test suite

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4) 24 Hours biasing

5) Post-radiation test + 24 Hours - including execution of the full TID test suite

6) 168 Hours annealing (biasing at 100^{o}C)

7) Post-radiation test + 192 Hours - including execution of the full TID test suite

3.8.6.3 TID Results Summary

No significant issues in the developed technology were detected during the TID radiation testing both for the digital and analogue parts of the circuitry. The functional tests after irradiation showed the same quality as before irradiation.

Static current tests after irradiation showed quite similar results as those before irradiation. A marginal increase in core supply static current was measured of a few percent, and in IO supply current an decrease of around 10% was measured. The measurement accuracy of the measured values with respect to voltage measurements (ATSTO) is ±2 mV, and with respect to the static current measurement is ±10 µA.

For the SerDes DC tests, the measured values are very much aligned before and after irradiation, exhibiting a difference usually within 1%.

It is therefore concluded that the designed circuit has a good level of resistance to total dose effects which shows the potential of developed technology for space applications.

3.8.7 SEL/SEU Testing

SEE testing was performed on the VHiSSI chip in order to receive first results of the behaviour during heavy ion irradiation. The SEL/SEU testing was carried out by Airbus DS and STAR-Dundee. Ramon Chips assisted with the analysis of the results.

3.8.7.1 Heavy Ion Irradiation Facility

The facility used for the heavy ion irradiation is detailed below.

Name: HIF UCL

Location: Université Catholique de LOUVAIN la neuve - BELGIQUE

Date: W42 2014

Characteristics: The CYClotron of LOuvain la NEuve (CYCLONE) is a multiparticle, variable energy, cyclotron capable of accelerating protons (up to 85 MeV), alpha particles and heavy ions. For the heavy ions, the covered energy range is between 0.6 MeV/AMU and 27.5 MeV/AMU.

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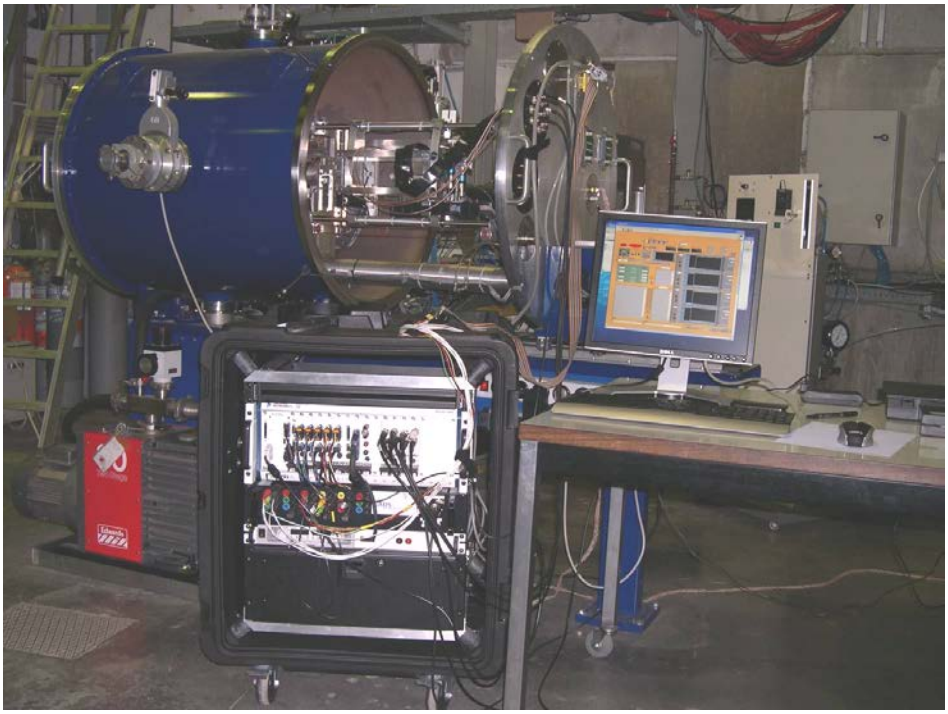

Figure 3-35 Photograph of the Irradiation Chamber

3.8.7.2 Description of the test system

The VHiSSI SEU/SEL test system is based on the VHiSSI LVDS board.

- A custom software in the computer allows to automatically configure the different registers inside VHiSSI and to control the test and monitor its status in real-time.
- The computer communicates with a SpaceWire Brick through a USB cable. The SpaceWire Brick allows creating SpaceWire packets that can then be sent to VHiSSI through SpaceWire Link 1.
- A special cable of 3 meter length was created, with a DB25 interface connection in the middle (i.e. 1.5 m cables are at each side of the DB25 interface). This interface is used to isolate the board and the chip inside the irradiation chamber while allowing the control and monitoring of the setup from the PC.
- The cable also featured two power lines of 3.5 V and 10 V to power the board and the latch-up protection circuit.
- This cable also provided a latch-up circuit reset outside the irradiation chamber. In case the maximum current limit is exceeded, the latch-up protection circuit activates and immediately disconnects the power supply in the board. It is manually operated, thus a switch shall be pushed to enable the supply again every time the protection circuit activates.
- The nominal SerDes is connected with a cable to a physical loopback (0.1 m).
- SpaceWire Links 2 and 3 are interconnected with a short SpaceWire cable (0.5 m).

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Figure 3-36 shows a diagram of the test setup.

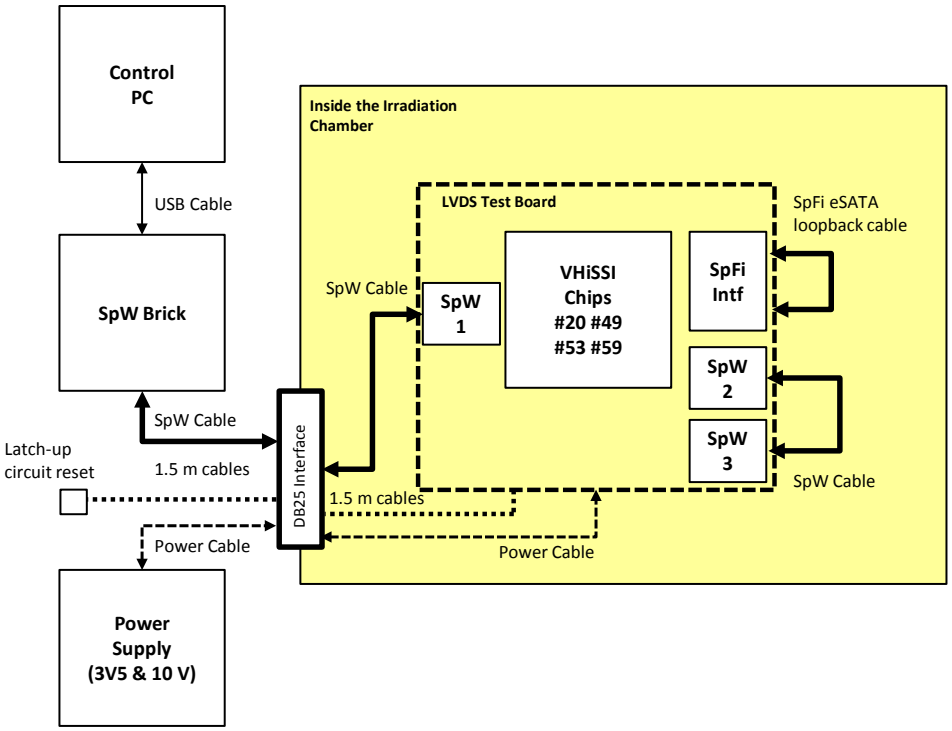

Figure 3-36 Test setup overview

Figure 3-37 and Figure 3-38 show the VHiSSI board mounted in the irradiation chamber. Once the chamber is closed a vacuum is generated. This guarantees that the right amount of radiation reaches the chip. On the left side of Figure 3-37 the cables are connected to the DB25 interface of the chamber. In Figure 3-38 the different connections detailed in the setup overview are shown. Note the different SpaceWire cable connections, SpFi cable connected to interface 0, the two power supply cables (3.5 V and 10 V) and the latch-up reset circuit. Also note the chip placed inside the socket located in the centre of the board. The plastic package has been removed, and through the hole in its centre it is possible to see the die exposed. This guarantees that heavy ions reach the target, impacting directly in the silicon.

Figure 3-39 shows the beam installation. The irradiation chamber is closed in this picture. The DB25 interface cable can be seen again at the top-left side (blue cables) where they are connected to the power supplies and SpaceWire Brick (not shown in the picture). The metallic pipe coming from a wall on the right-centre of the image carries the radiation inside the chamber.

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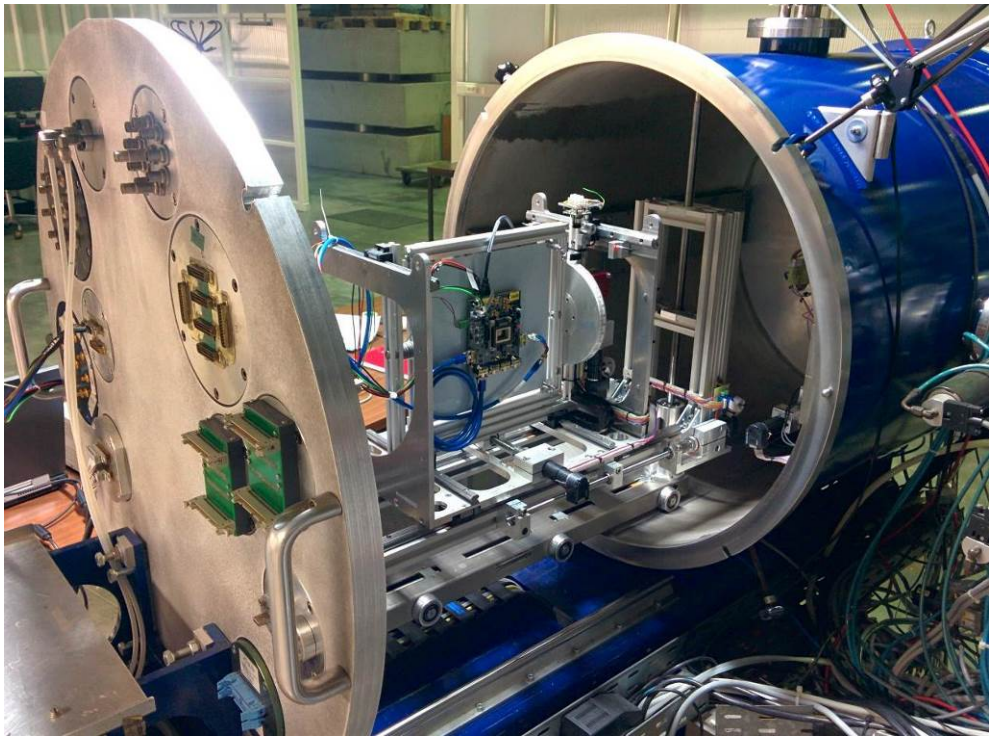

Figure 3-37 VHiSSI Test Board Mounted in the Irradiation Chamber Support

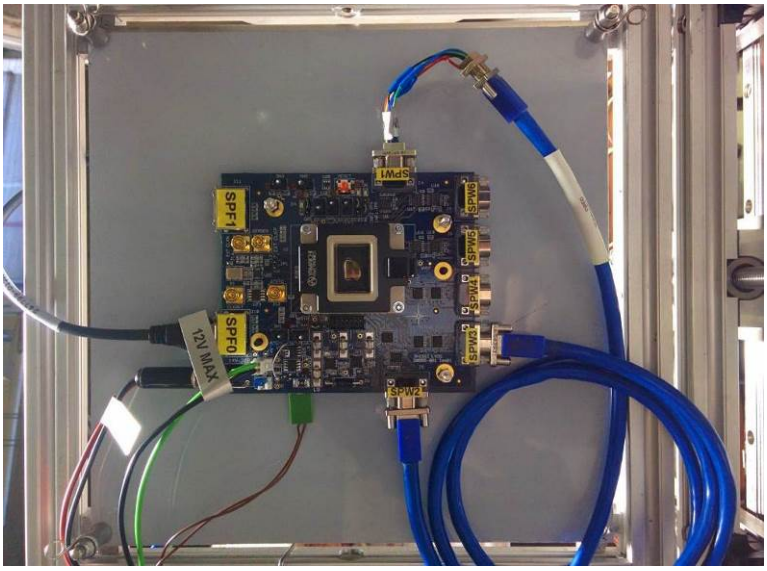

Figure 3-38 Close Up of VHiSSI Test Board Mounted in the Irradiation Chamber Support

The research leading to these results has received funding from the European Union Seventh Framework Program (*FP7/2007-2013*) under grant agreement no. 284389

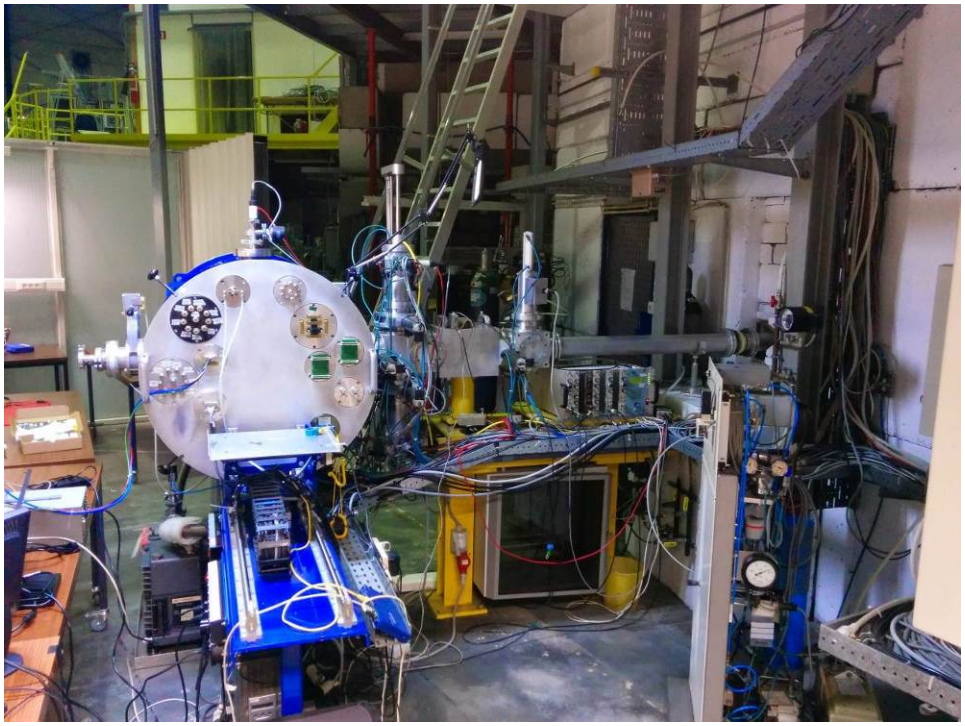

Figure 3-39 Irradiation chamber and beam installation

The die of the different chips has not been completely exposed. The selected VHiSSI plastic package does not allow easy removal of the lid. A chemical process is required. This chemical process is aggressive and must be carefully controlled not to damage the chip. From the original 5 chips sent for lid removal, one chip (#15) had its bonding damaged. Consequently, extreme care was taken not to damage any more chips. The final degree of silicon exposure ranged from 93% to 97% for the four functional chips (see Figure 3-40).

The tests performed involved the four remaining VHiSSI chip samples. All of them were tested but the ion cocktails applied were different. On the first testing day VHiSSI chips #59 and #53 were tested using the same ion cocktail. On the second testing day VHiSSI chips #20 and #49 were tested using a different radiation cocktail than the first day.

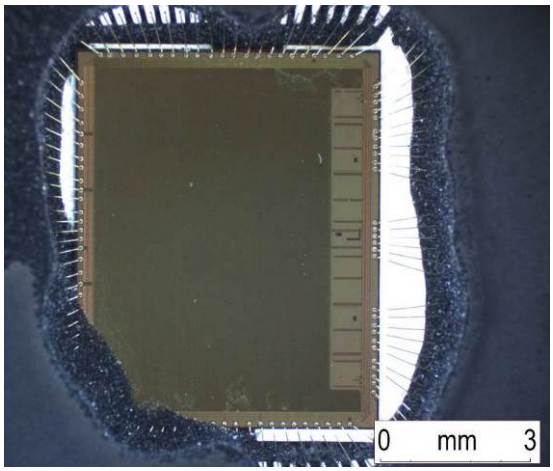

Figure 3-40 VHiSSI chip with lid removed

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3.8.7.3 SEL/SEU Results

During the SEU tests of VHiSSI chip, carried out by Airbus DS and STAR-Dundee in Belgium's ion accelerator, instant increase of current on the chip was observed. The current step was ~300mA, which was seen during the operation and powering of the chip. The device was operating properly when no ions had been accelerated into the chip, and these effects had been seen only when the ions had been accelerated.

Such a dramatic increase of current might be related to one of the below issues:

- Latch-up of internal circuit in VHiSSI
- Latch-up of VHiSSI I/O
- Latch-up of VHiSSI SerDes
- Contention between VHiSSI output buffers and other devices (FPGA) on the test board

Unfortunately, the tests had been done without the ability to monitor each one of the power domains individually. Such separation could enable immediate and reliable pinpointing at the root cause of the problem. As a result, the confidence level of the following arguments is not complete, and should be considered as assumptions with high confidence level.

It is thought that this phenomenon may be caused by one or more of the following possible causes:

- Latch-up of VHiSSI I/O
- Contention between VHiSSI output buffers and other devices (FPGA) on the test board
- Latch-up of VHiSSI SerDes
- Latch-up of internal circuit in VHiSSI

Latch-up in internal logic is unlikely because internal logic runs at 1.2V Vdd and is least susceptible to latch-up.

If VHiSSI I/O became latched-up during irradiation, they may also be sensitive to latch-up that may be caused electrically by external voltage and current circumstances. To investigate this possibility, Ramon Chips conducted IO Latch-up Tests in a test house (Presto Engineering, Israel), which showed no sensitivity of the VHiSSI chip to latch-up.

The SEE tests revealed a problem with the radiation tolerance of the VHiSSI device. Analysis of the possible cause of this problem is underway, but is not yet complete. For an additional SEE test campaign a detailed failure mode measurement should be performed. SEFIs should be observed without any latch-up protection in a repeat cycle to see any accumulative effects like increase of the power supply current or any destructive behaviour.

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3.8.8 VHiSSI Chip Test Results Summary

The VHiSSI chip has been extensively tested and validated. The SpaceFibre interface in the VHiSSI chip is capable of operating as designed at 2.5 Gbits/s with 11 virtual channels. It has 10 SpaceWire links that can operate at 200 Mbits/s, a FIFO interface that operates at 62.5 MHz, a memory interface that also operates at 62.5 MHz and a DMA interface whose performance is limited by that of external memory and is able to operate at 31.25 MHz. The VHiSSI chip supports the SpaceFibre QoS which successfully provides priority, bandwidth reservation and scheduled qualities of service. The VHiSSI chip was tested under total ionizing dose radiation and no significant radiation induce effects were observed.

Experimentation with the tested VHiSSI chip confirmed its operation as a SpaceFibre interface to a high data-rate instrument. Using the FIFO mode of operation VHiSSI was able to transmit data from a simulated instrument in an FPGA attached to the VHiSSI chip using the FIFO interface over one virtual channel of the SpaceFibre interface at almost 2 Gbits/s. At the same time it was able to receive commands and provide housekeeping information using a second virtual channel of the SpaceFibre interface. The VHiSSI chip is able to operate as a small, low power, effective interface to a high data-rate instrument.

The VHiSSI chip when operating the SpaceWire LVTTL mode was able to take data from one SpaceWire interface operating at 100 Mbits/s and a further ten SpaceWire interfaces running at 200 Mbits/s and concurrently send the information from each SpaceWire interface over a separate virtual channel of the SpaceFibre interface. Furthermore it was able to do this while at the same time receiving the same volume of data over each of the SpaceFibre virtual channels and sending it out of the corresponding SpaceWire interfaces. The VHiSSI chip is able to operate as a SpaceWire to SpaceFibre bridge device providing up to 11 SpaceWire LVTTL interfaces or up to 5 SpaceWire LVDS with one LVTTL interface, with the number of LVDS interfaces being programmable from 0 to 5.

The experimental SpaceFibre High-Speed Serial Interface or VHiSSI chip was a substantial success, however, a number of issues were identified during the testing which need to be resolved before the chip and related technology can be exploited. These issues are summarised below:

Design Errors: There were a number of design errors which are straightforward to fix now that they have been identified:

Manufacturing Issues: The early use of the RADIC 5 test chip helped remove many manufacturing and design issues. There are, however, still some manufacturing issues with the VHiSSI chip. The results from this work have been used to improve the process prior to it becoming a commercially qualified process. The fabrication of RADIC5 and VHiSSI ASICs contributed significantly to the improvement of the IHP process and design kit. The early exploration enabled the improvement of the CMOS transistor model and finding of the problems with capacitive load mapping. Moreover several bugs in design kit have been identified and after that corrected. First fabrication of RADIC5 was followed by the large spread of the static current in different chips. It was assumed that density rule violation is the cause for this problem and this was confirmed over VHiSSI chip where this DRC issue

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was avoided and fabricated chips reported very low spread in the static current consumption. The design rule has been established as a part of acceptation/rejection process of the chips for tape-out. The experiences of VHiSSI project also contributed to decision to establish yield measurement vehicle which will be present in each multi-project wafer (MPW) run and serve as an indicator for the yield for each produced wafer.

Radiation Testing Issues:

Radiation testing had been carried out on the RADIC 5 device and the results used to improve the design and manufacturing process. Both TID and SEU/SEL radiation testing were carried out on the VHiSSI device. The TID resting showed good immunity to radiation, however, the SEU/SEL testing discovered a significant issue with a SEFI. Further testing indicates that this is not a latch-up but some other effect.

The VHiSSI chip functions well and has been demonstrated in its major operational configurations. It meets its performance targets. There are a number of minor design issues which can be resolved easily. The number of functional devices was low, but the VHiSSI project has helped to improve this new process from IHP and further improvements based on the VHiSSI chip are being put into effect. The SEU/SEL issue observed is a significant issue which is currently being investigated by the relevant members of the VHiSSI team. The TID testing showed excellent resilience to TID radiation.

3.9 VHiSSI Objectives Addressed

The VHiSSI research programme has researched, designed and developed an experimental high speed serial interface device, VHiSSI, which:

- Provides multi-Gbit/s serial data-link technology, essential for future spacecraft onboard data-handling systems.
- Levers prior and concurrent research on the emerging SpaceFibre standard, to provide a complete multi-Gbit/s serial technology for spacecraft onboard data-links and networks, including fault detection, isolation and recovery (FDIR) and quality of service (QoS).
- Provides a versatile chip architecture, which can be adapted and configured to support multiple applications.
- Provides the critical clock-recovery mechanism on existing European chip technology.
- Uses a European semiconductor fabrication facility, enhancing and developing its capabilities for radiation tolerant chip design and production with a radiation tolerant library. Further work needs to be done related to the SEE testing.
- Provides a non-dependent technology allowing unrestricted use on European spacecraft and substantial export opportunities - an important capability for Europe.

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4 Potential Impact, Main Dissemination Activities and Exploitation of Results

4.1 Potential impact

The impact of the VHiSSI research is a very high-speed network technology for future telecommunications and Earth observation spacecraft, with terrestrial avionics, robotics, automobiles and other applications also expected to benefit.

The principal benefits of the VHiSSI research programme are:

- Very high-speed serial-interface technology applicable to many space missions, including large and small satellites, robotic missions, planetary landers and rovers, launchers and related EGSE, and which is capable of spin-out to a wide range of terrestrial applications, including demanding robotics applications.
- A high-speed serial interface chip implemented using a radiation-hard standard cell library optimized for a new 130 nm CMOS process, although further work needs to be carried out related to SEE.
- Mixed-signal high-speed radiation-hardened integrated circuits that are free from international export restrictions (non-dependent) that are fabricated and tested in Europe, and that are available to members of the European Union for use in space missions. The SEE issue detected in the last month of the project needs to be addressed.

The medium term impact of the VHiSSI programme will be an independent European technology for spacecraft high-speed data-links and network technology. The VHiSSI research has laid the technological foundations for a complete spacecraft onboard data-handling solution, saving mass and power, improving reliability, and substantially simplifying complex system design.

Space-based Earth observation and scientific instrumentation currently under development will push the limits of on-board data-handling technology. Several future space-based instruments, for example synthetic aperture radar (SAR) and hyper-spectral imagers, will be capable of producing data at data rates of several Gbits/s. Telecommunications satellites also have to handle many Gbits/s data on-board. To support the growing demand for on-board communications network bandwidth, ESA has been developing a standard multi-Gbits/s network technology called SpaceFibre. At present this important ESA technology is dependent upon the USA for the radiation-tolerant physical layer devices. USA International Trade in Arms Regulations (ITAR) severely restricts the use of these technologies on European space missions.

The main objective of the VHiSSI research programme was to create very high-speed data-interface technology. Levering prior and concurrent research on the emerging ESA SpaceFibre on-board communication standard, it would provide a complete solution for spacecraft on-board data-links and

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networks. It would also provide a non dependent (ITAR free) technology, allowing unrestricted use on European spacecraft and creating substantial export opportunities. Non space applications expected to benefit from the anticipated technological advancements and resultant European capability include terrestrial avionics, robotics, and automobile networks.

The VHiSSI project has integrated a complete SpaceFibre protocol engine, together with the physical layer interfaces, in a radiation tolerant chip manufactured by a European foundry. Not only does this alleviate the dependency on very high-speed serial interface devices, it provides a complete SpaceFibre solution in a single chip. In the process of developing the VHiSSI chip an important European radiation-tolerant ASIC fabrication capability has been demonstrated. The VHiSSI research programme has created a very high-speed data-interface technology which is a critical component technology for future spacecraft payloads, particularly telecommunications and Earth observation payloads where multi-Gbits/s data-rates are urgently needed. A complete solution to very high-speed data networking onboard spacecraft has been provided, levering research on SpaceFibre, using a European fabrication facility, and providing a non-dependent technology. An experimental SpaceFibre interface device (VHiSSI) has been designed to connect instrument electronics and other spacecraft equipment to SpaceFibre and also to bridge between SpaceFibre and several SpaceWire devices.

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- Levers prior and concurrent research on the emerging SpaceFibre standard, to provide a complete multi-Gbit/s serial technology for spacecraft onboard data-links and networks, including fault detection, isolation and recovery (FDIR) and quality of service (QoS).
- Provides a versatile chip architecture, which can be adapted and configured to support multiple applications.
- Provides the critical clock-data recovery mechanism on existing European chip technology.
- Uses a European semiconductor fabrication facility, enhancing and developing its capabilities for radiation tolerant chip design and production with a radiation tolerant library. Further work needs to be done related to the radiation single event effects (SEE).
- Provides a non-dependent technology allowing unrestricted use on European spacecraft and substantial export opportunities - an important capability for Europe.

The VHiSSI project will have a positive economic impact on the SME and industrial partners who have been involved in the project. The partners are already planning to commercially exploit the results of the VHiSSI project through new or improved products and services which will be available over the next 4 years. The SME partners also expect this will have a positive impact on employment resulting in approximately 2 new jobs.

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The VHiSSI project will also have an educational impact with the University of Dundee Space Technology Centre planning to incorporate elements of the project results into their undergraduate and postgraduate courses.

4.2 Main dissemination activities

Dissemination took the following forms:

- The VHiSSI project WEB site;
- Participation in SpaceWire Working Group meetings and scientific conferences;
- Publications.

The VHiSSI website (www.vhissi.eu) provides information on the project for both the general public and the research community. The **Project** page describes the background and aims of the project and the **News** page contains links to the project progess reports and news articles related to the project partners. The **Publications** page is aimed more towards the research community and contains details of all project-related papers presented at scientific conferences.

Over the course of the project, a number of the VHiSSI partners have been involved in presenting the key features and concepts of VHiSSI and SpaceFibre at a wide variety of forums. This included the SpaceWire Working Group meetings, two International SpaceWire conferences and ten scientific conferences in Europe, the Middle and Far East and North America. The SpaceWire Working Group meetings provided an important vehicle for gaining feedback and validating the future plans at each stage of the project and enabling early engagement with the end user community.

The majority of the papers presented at the scientific conferences have also been published in the associated conference proceedings. The **Publications** page on the VHiSSI WEB site contains links to the relevant conference proceedings.

4.3 Exploitation of Results

The results of the VHiSSI project will be exploited by the VHiSSI partners in several of ways:

The SME and industrial partners plan to develop new products and/or services and enhance their existing products and/or services based on the knowledge gained from the VHiSSI project.

STAR-Dundee Ltd will commercialise the VHiSSI technology it has developed, using the digital VHDL designs in both ASIC and FPGA implementations of SpaceFibre. A SpaceFibre evaluation, development and test board that provides the SpaceWire to SpaceFibre bridging capabilities of the VHiSSI device is currently being specified and will be developed by STAR-Dundee over the next four-six months. This will be an important member of a family of SpaceFibre development kit being planned by STAR-Dundee. The results of the VHiSSI project will also feed into the design of the STAR-Dundee's SpaceFibre IP core; improving its performance and enhancing its capabilities.

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STAR-Dundee have used the experience in designing a high performance ASIC gained during the VHiSSI project to improve the SpaceFibre IP core previously developed for ASIC implementation. In addition, STAR-Dundee's employees are much more knowledgeable about the entire chip design process and therefore are more readily able to support customers of their SpaceFibre IP cores.

ACE-IC has designed an effective SerDes in a radiation tolerant technology, with very good performance in the target technology. ACE-IC will include this design and the related knowledge and experience gained on the VHiSSI project in their product portfolio.

Ramon Chips will use the methodology and set of design rules developed for third-party designers of custom-designed analog/mixed signal circuits with I/O to assure radiation hardness in future similar collaborations.

Ramon Chips will use the know-how and technology regarding the integration of a high-speed SerDes block into digital rad-hard chips in future products that will incorporate similar or even more demanding SerDes components and other mixed-signal components.

Ramon Chips will apply the know-how and technology regarding the packaging and assembly challenges posed by very high-speed serial links in future projects and products which may include SerDes and other high speed interfaces.

IHP will use the enhancements to their 130nm Process Design Kit (PDK) in all ongoing academic and commercial projects aiming for ASIC fabrication.

Future Research

A number of the VHiSSI partners plan to use the results of the VHiSSI project in future research activities.

The results of the VHiSSI project will be used in many aspects of research in the Space Technology Centre at the University of Dundee. The VHiSSI chip will be used as an exemplar of SpaceFibre technology and help promote this important European technology for future space flight applications. The University of Dundee will use the VHDL code and test boards developed by STAR-Dundee in the University's future research. SpaceFibre is of growing interest in the international space community and the VHiSSI research has helped place University of Dundee at the forefront of that technology research.

IHP have been working on the development of new methodology and architecture for radhard circuit, which has resulted in 4 published papers. IHP will continue research in this area using the knowledge gained from the VHiSSI project.

Education and Training

SpaceFibre will be used as an example of a high-performance network technology within the "Research Frontiers" final year undergraduate computing course at the University of Dundee and the VHiSSI chip will be used as an example of an advanced SpaceFibre device. Postgraduates and Internees within the University of Dundee Space Technology Centre will also receive training on

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SpaceFibre and have the opportunity to use a VHiSSI chip for research purposes. Training on SpaceFibre will also be given to aerospace industry engineering staff, again using VHiSSI as a stimulating example of a SpaceFibre chip. VHiSSI is expected to be a very useful case study in both undergraduate and post-graduate courses.

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5 Project Details

Title	**VHiSSI: Very High Speed Serial Interfaces** (GA no. 284389)
Coordinator	**Prof Steve Parkes,** **The University of Dundee**, United Kingdom
Consortium	**STAR-Dundee Limited,** United Kingdom **RAMON chips Ltd**, Israel **ACE-IC Limited**, Israel **IHP**, Germany **Airbus DS GmbH**, Germany **SYNERGIE CAD INSTRUMENTS s.r.l**, Italy
Duration	1 January 2012 – 31 October 2014 (34 months)
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Budget	EU contribution: 1,999,998.98 €
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