FINAL REPORT

SP1-JTI-CS-2013-03

Project Acronym:	FUSES 2014
Full Title:	Current Limiting Device to Address DC Aeronautics Power Distribution Systems
Project no.:	641336
Managing institution:	MERSEN SB SAS
Due date of report:	20/08/2016
Start date of the project:	01/09/2014
Duration:	24 months

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1. Executive summary

Electrical Power Distribution Systems (EPDS) employed among others in Aeronautics are usually protected by active electronic driven switching components. In order to reduce response time and simplify protection driving, fuses are being considered as one of the prerequisite for the CleanSky HVDC network.
The development of a new generation of hybrid and/or full static current limiter solutions, able to operate above 51000ft, is crucial for specificities of aircraft applications. From one side fuses technologies could be adapted to parts of the requirements but may not fully comply. On the other side, the material properties of Silicon Carbide as semiconductor, clearly superior to those of Si, should lead to enhanced hybrid current limiters with much better performance than conventional fuses or Si based solutions.
Pooling leading fuses and protection devices manufacturer, and two research groups, FUSES 2014 aims at a breakthrough in current protection technology to build either a hybrid and/or a full static current limiter solution with different benefits than existing solutions. Well stablished and new methodologies will be adapted to fuses and SiC technologies and optimized to make them a practical reality.
The main targets are study, optimize two solutions and validate the optical module following DO160 standard adapted to high DC voltage networks to be integrated into aircraft EPDS:

- A required specs Silver fuse and specific package.
- A SiC current limiter using existing SiC FET technologies plus its optimal packaging configuration.

Our goal is to demonstrate the innovative character of our proposal by studying technologies that can meet the bill of requirements base on 60 years plus of current limiting device by Mersen with the support of 2 well-known universities that have demonstrated a thinking out-of-the-box in the field of current limiting devices.

We believe that for example SiC brings the plus that move current limiting device to hybrid and/or full static current limiting device. Taking into account the initial specifications listed in the call for proposal SP1-JTI-CS-2013-03-SGO-02-066, there is no existing product available on the market and specific development must be carried out to reach the objectives. The nearest fuse available is a NA UL Class T fuse, A3TX, X been the current fuse rating. The rating has been determined by taking into account the application bill of requirements.
A comparison of the performances reached by the different DC current limiting devices is shown in the following table (Table 1):

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DC current limiting device	Response time T(3 In) < 3s T(10 In) < 10 ms	Response time I=11kA T<320 us	On state Vdrop<125 mV For In=83A	Reliability 10 years	Temperature 95°C – 125°C
DC Breaker	Limited for DC	Not possible	Good	Good	Good
Fuse	To be designed	Good	Good	To be verified	To be verified
Pyrotechnic	Difficult to achieve	Difficult to achieve	Good	To be verified	To be verified
Superconductor	To be designed	Not possible	Good	To be verified	Superconductor temperature: -200°C
SiC Current limiter device	Good	Good	Not possible Ron= 80 mΩ	To be verified	Good
Hybrid	Good	Good	Good	To be verified	To be verified

Table 1. Comparison of the performances reached by the different DC current limiting devices

As no obvious solution is available, we have studied two of the previously mentioned technologies, mainly Fuses and Hybrid current limiters. For this purpose, we have adapted the existing Mersen fuse technology to develop a new fuse in accordance with the specifications or part of the specifications. In parallel, we have studied and developed a Silicon Carbide current limiter based on a power FET technology with two (ACCUMOS) or three electrodes (JFET).

The innovative character of this project proposal resides in the association of this current limiter with the developed fuse to build a hybrid current limiter solution. For the 2 types of technologies, the ON state, the clearing state and the OFF state have been closely studied. For example during the ON state the voltage drop has to be minimized, clearing state the energy dissipated by the device has been considered and for the off state leakage current has been taken into account. The specificities of aircraft applications have been taken into account, especially regarding altitude working conditions (51000ft).

Then, the main objectives can be summarized as follow:

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1. Study and optimize a Silver fuse with specs as much as required and specific package for aircraft working conditions.
2. Study and optimize a SiC current limiter using existing SiC FET technologies
3. Study an optimal packaging configuration for hybrid solution fitting with altitude working conditions among others
4. Test of fuse and hybrid solutions and main parameters extraction
5. Validation of the optimal module following DO160 standard

2. Summary description of the project context and the main objectives

2.1 WP1. Fuse module optimization and fabrication

The objectives of this work package are the dedication of the design and optimization of a fuse module fitting as much as possible with starting specifications. The base technology used has been the Mersen silver technology. New dimensions and geometries have been considered to fit with the required current.

2.1.1 Task 1.1 State of the art review and analysis of specification

As starting point, a state of the art review of existing aeronautics fuses and current limiting solutions has performed. On state specification, fault current available in the DC circuit, time current curve needed to meet bill of requirement has been studied to draft a technical solution. The strategy to be used for the study has been set-up. This strategy has impact in both WP1 and WP2.

2.1.2 Task 1.2 Geometry design and optimization of the fuse

The consortium experience in the fuse element design permits to shape the time current curve in order to meet certain gates. The goal is to design a fuse element with a new reduce sections area that allows to test the new design against the bill of requirement. Simulation means, as well as testing means, have been used to verify the fuse design.

2.1.3 Task 1.3 Fuse module fabrication

In the previous report, we have seen the design of a fuse against the bill of requirement. MERSEN experience in the fuse element design allows shaping the time current curve in order to meet certain gates. Simulation has been used to verify the fuse design. After test analysis of the first fuses batch, a redesign will be considered for the second production batch.

2.2 WP2. Semiconductor fuse design and fabrication

The objectives of this work package are the dedication of the design and optimisation of a SiC semiconductor current limiter fitting as much as possible with starting specifications. The base technology used has been the CSIC JFET technology, previously developed and tested by the project partners. New

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devices dimensions and geometries have been considered to fit with the required specifications. Some process technology adjustments have also been necessary.

2.2.1 Task 2.1 Analysis of specification

The starting specifications have been analysed and compared with the performances of existing SiC current limiter developed by the 3 project partners in previous works. From this initial analysis, several optimisation axes have been defined for the next phase of design and optimisation of the targeted device. This analysis has been done by all 3 partners.

2.2.2 Task 2.2 Geometry design and optimization of the current limiter

In this task, 2D simulation work with numerical simulator has done by INSA Lyon in order to adjust the device basic cell geometry of the device to the specs. The possibility to change some doping or etching profiles in the technology has been consulted to CSIC partner. Once defined the basic cell geometry, both INSA Lyon and CSIC have drawn the photolithography masks set using common software. Current limiter as well as technological and electrical test structures is included on the mask set.

2.2.3 Task 2.3 Technology optimization and device fabrication

Some preliminary processing tests have performed in order to adjust possible doping or etching profiles changes defined in task 2.2. Once the photolithography mask set available from task 2.2, device fabrication have started in the CSIC clean room.

2.2.4 Task 2.4 On-wafer characterisation of the current limiter

Once completed the clean room processing, a basic on-wafer characterisation of the fabricated devices will be performed. From this characterisation phase, good dies will be identified for packaging.

2.2.5 Task 2.5 Devices packaging

Dicing and die selection will be done by the partners. Taking into account the specific requirement of the application in term of pressure, temperature, humidity and mechanical stress, part of the packaging of the SiC device will be subcontracted, and part will be done by the partners

2.3 WP3. Module characterization and validation

The objective of this work package is to validate one of the 2 proposed solutions for the module, which are fuse or current limiter hybrid module. For this purpose, the consortium are working since M10 on a standalone characterization and engineering tests of each 2 solutions before selecting the most adequate.

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2.3.1 Task 3.1 Fuse module standalone testing

Mersen DC labs in Europe and US allow the consortium to speed up the testing. Due to the availability of the lab different fuse solutions are tested and the results will be evaluated against the bill of requirements. Mersen is already supplying products qualified with DO160 standard to aeronautics industries and own the facilities to perform electrical and environmental engineering tests.

2.3.2 Task 3.2 SiC current limiter hybrid module testing

The labs of the three partners will be used to make a full testing, including engineering DO160 testing, of the SiC current limiter hybrid module. Most electrical testing will be done by INSA Lyon and CSIC while the environmental testing will be performed by Mersen.

2.3.3 Task 3.3 Final optimal module testing

In a similar way to task 3.1 and 3.2, the final module selected as optimal solution will be tested to extract the main parameters and to demonstrate DO160 standard validation.

2.3.4 Task 3.4 TRL validation and support to integration in EPDS demonstrator

The final modules will be produced and delivered by Mersen to the clean Sky partners in charge of EPDS demonstrator. Mersen will support the integration of the modules in the final demonstrator.
All the partners will assess the Clean Sky partners on the testing of the modules.

2.4 WP4. Management, exploitation and dissemination

The objective of this work package is to efficiently execute legal, contractual, ethical, financial and administrative management of the project, the grant and consortium, so as to facilitate R&D, validation and dissemination activities by allowing researchers and industrial partners to focus on adding S/T and market value.

2.4.1 Task 4.1 Management

This task covers activities related to the overall organization, planning and control of the project. It addresses liaison with the Commission and the Clean Sky platform, ensures timely delivery of deliverables as well as any other contractually relevant document and includes:

- The overall legal, contractual, ethical, financial and administrative management;
- Management of all financial aspects, including European contribution and auditing and also will monitor and assure the timely and quality project reporting (Periodic Reports).

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- The scientific and technical co-ordinator will also be responsible for the technical coordination of the management & technical tasks of the project
- Coordination of knowledge management and other innovation-related activities

Management includes effective decision-making procedures, optimum internal communication, conflict resolution and active promotion of collaborative work among researchers' teams.

2.4.2 Task 4.2 Explotation

The results from this project will be used to expand partners´ product portfolio to include new fuses and limiting systems for aircraft application. Concerning Standardization, devices will be tested following DO160 standard within the project. However, the project partners will also consider if new test methods for the product qualification need to be developed as complement to the existing standards. In case of positive answer, a report on such possible alternative testing methods would be generated. To strengthen the project IPR strategy, early activities will be dedicated to a patent mapping review. The mapping activity will identify existing patents that match closest to the project innovations, thereby: (1) enabling the innovative claims of the project to be strengthened (better defined); (2) helping to identify competitive technologies and free patent space; ensuring protection of the project results; and (3) helping to identify wider opportunities for exploitation. It is important to note that the partners already share common patents in the field.

2.4.3 Task 4.3 Dissemination

Dissemination of the project results will be carried out using the following channels: participation to Clean Sky events and in topic related conferences, production of papers/articles and press release. The presence of two academic partners will help the dissemination at scientific journals and conference levels. Reference to Clean Sky project will be done in the acknowledgments. The coordinator will be in charge of dissemination in Industrial forums (PCIM…), in free specialized journals such as Bodo Power or EPE journals, and through press release.

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3. Description of the main S & T results/foregrounds

3.1 WP1. Fuse module optimization and fabrication

3.1.1 Task 1.1 State of the art review and analysis of specification

D1.1 Report on existing aeronautics fuses state of the art review

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3.1.2 Task 1.2 Geometry design and optimization of the fuse

MS1 Preliminary design review

The objective of the Clean Sky project is to implement a power distribution in aircraft instead of hydraulic and thermal systems. This change will allow reducing volume and weight. In this project, the electrical system is a continuous transmission line. MERSEN expertise involves in the current limiter protection.
Whose specifications are the following ones:

- Nominal bus voltage = 540V with Vbus max= 900V
- Maximum voltage drop at 90°C Vdrop=125mV

- Nominal current In = 83A
- Maximum leakage current Ileakage= 100 uA

- Overshoot : Iover= 120 A et Vover= 650V during 60s

- Melting time :
  - 250A → 3s
  - 830A → 10 ms

- L/R < 5ms

- Temperature:
  - Device = 95°C (between -40°C and 130°C)
  - 130°C during 1h without degradation
  - -40° C during 1h without degradation
  - 150°C during 5 min without degradation
  - -50°C during 5 min without degradation

- The lifetime should be superior to 10 000 cycles

The goal is to design a fuse element with a new reduce sections area that will allow testing the new design against the bill of requirement. The fuse is the most reliable breaker. It is a pure thermal device that will clear the circuit when the fault current has created enough energy to melt its conductive element. Large power fuses use conductive elements made of silver, copper or tin to provide stable and predictable performance. The structure of the fuse is shared in four elements: electrical connection, fuse element (conductive element), extern isolation (ceramic) and sand.

The simulation of the new fuse has been established and the optimization of the reduced section allows shaping the time current curve in order to meet certain gates.

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MS2 Critical design review

The optimization could be reached by changing the reduced section. The reduced section located in a fuse, contributes to:

1. <u>The conductive behaviour:</u>

   In case of nominal current, the fuse must allow the current flowing with a minimal resistance. This current provides a thermal effect which must be low.

2. <u>The switch off behaviour:</u>

   In case of over current (Fig. 2), the reduced sections melt because of the Joule effect heat. An arc is created in the fuse element. This arc grows up and consumes the fuse element.

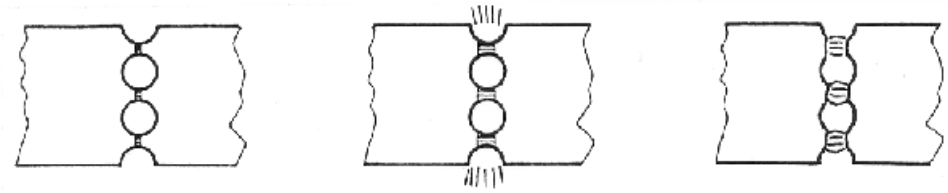

Figure 2. The switch off behaviour with over current

It seems obvious that the arc must be contained to avoid an overextension. The aim is to stop the current flow as fast as possible and reduce the created energy diffused in the fuse.

Thus, the dimension and the shape are decisive to find a compromise between the conduction and the switch off.

The matrix 13260 and 19449 are the fastest dies. These results show the influence of the matrix geometry on the curve time/current.

The impact of the surface influences the heat evacuation. The curve shifts on the right and the fuse is faster (All results are presented in D2.1).

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3.1.3 Task 1.3 Fuse module fabrication

D1.2 Fuses prototype gen I delivery

Prototypes (see Fig. 3) have been realized and the presentation of the manufacturing process control and test will be written in the following deliverable D3.1 (to be delivered on Month 14).

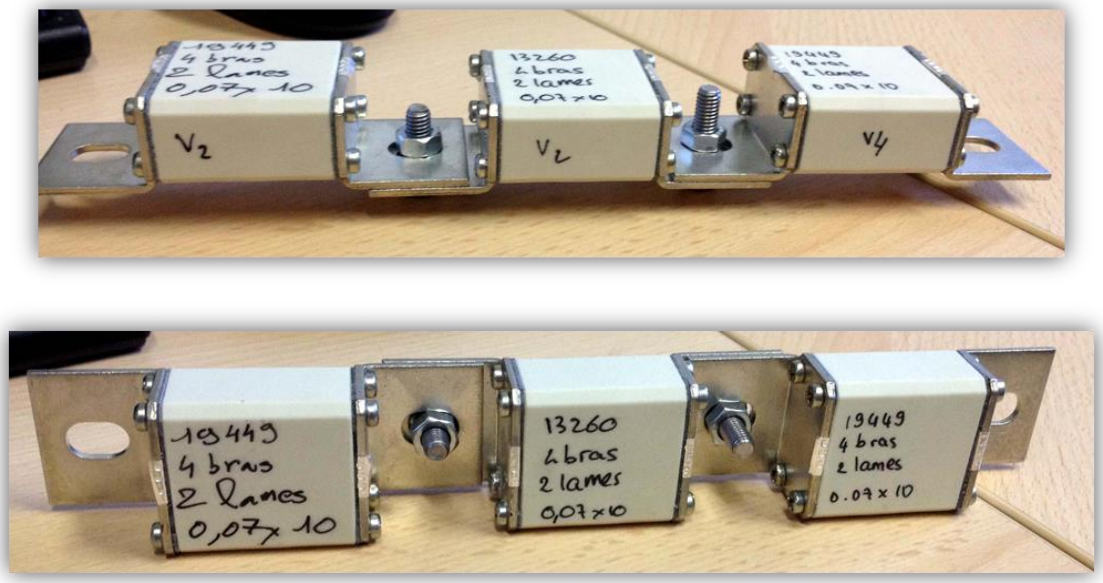

Figure 3. The fuses prototype gen I

Prototypes have been made in MERSEN with two different matrixes. And the simulation of the fuse has been done. Its simulations are summarized in Table 2 (see **2.7.1 MS3 Start fuses I testing**).

D1.3 Report on existing aeronautics fuses state of the art review

This paper presents a novel solution based on a hybridization of fuses and pyroswitch components that may answer new DC protection needs.

Pyroswitch

The pyroswitch is an electrical interrupter and, in contrast to a fuse, the time to achieve a complete disconnection of a circuit will not be dependent on the magnitude of the over current. In general, a pyroswitch utilizes a miniature guillotine that is propelled by a pyrotechnic charge to achieve the force required to cut through a metal conductor (busbar) as described in figure 2. This gives a very simple and thus extremely reliable behavior. The pyroswitch has no impact on the electric system before operating since it is positioned above the busbar. After operation, it cuts the busbar and separates/isolates the two conductors. The cut-off time is lower than one millisecond. Figure 2 presents a sectional view of a pyroswitch developed by Herakles Safran. The copper bar is depicted in orange, the initiator is illustrated in yellow and the blue part represents the guillotine.

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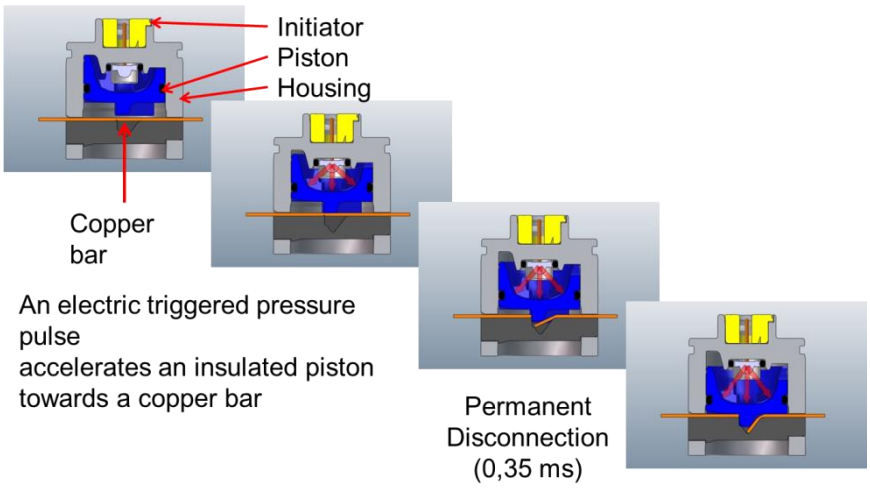

Fig. 2: Sectional view of a pyroswitch

A pyroswitch alone is compatible with medium power devices (electric device) at I ~ 400 A and V ~ 50 V. Any increase in the current range requires increasing the section of the busbar, thus increasing the energy in ignition required for disconnection. Similarly, any increase in voltage will require more distance between the conductors after the busbar is cut, and thus complicate the device and make it bigger.

Even if a pyroswitch has the advantage that it is faster operating than a strictly mechanical apparatus and is much less expensive than are purely electrical breakers in high load applications, this kind of device suffers from several drawbacks. Notable among these is the risk of harmful arcing when cutting off an inductive circuit. A simplified explanation for this is that the circuit with inductive current is reluctant to change. This reluctance causes a harmful arc between two formerly connected conductors at the moment of disconnection. In contrast to the type of “soft” arc that appears anytime when a circuit with no inductance (i.e. a capacitive circuit) is disconnected, an arc under influence of inductance will not be easily extinguished. While the reasons for these deficiencies are not straightforward, the failure in the pyro breakers under high loading may be due to their inability to rapidly turn off the ionization between electrode parts.

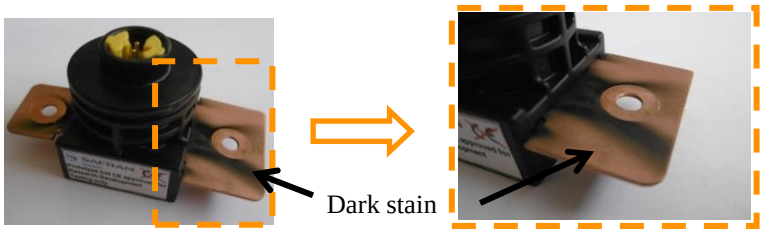

Fig. 3: Pyroswitch pictures after a loading test (200V-250A-L/R=200µs)

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Preliminary tests have been done on a pyroswitch alone to understand the limitation of the ability to protect a DC system. The first test was a 200V, 250A with a very low L/R of 200 µs. Figure 3 shows pictures of a pyroswitch after a loading test. The device has cut off the circuit but a dark stain has appeared on the copper bar, due to the reluctance. The breakdown voltage after the test was also abnormally low (dielectric test =500V). Another test with a lower voltage of 150V has been performed and the breakdown voltage after the ignition was as expected (i.e. >5kV). Thus 150V seems to be the limitation of this pyroswitch.

It is therefore one object of this paper to provide a high speed, high voltage hybrid OCP device capable of minimizing system exposure to circuit faults.

Hybrid solution: Pyrofuse

This section presents a new hybrid protection solution, in which a pyroswitch element and a fuse element are configured electrically in parallel. Figure 4 shows the pyroswitch (grey) and the fuse (white). The parallel configuration means the designer can choose the best components of each type. Indeed, the fuse and the pyroswitch interact with each other. This section presents the steps in their behavior.

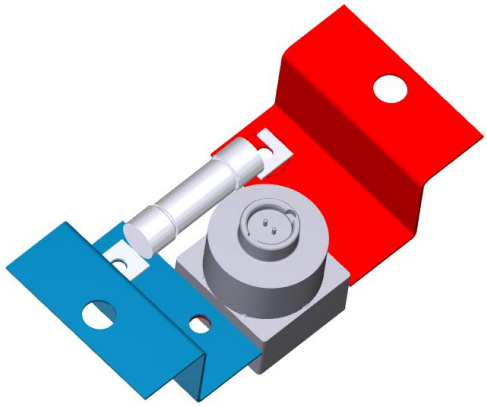

Fig. 4: New hybrid protection solution with pyroswitch and fuse in parallel

Figure 5 presents the electrical schematics of the pyrofuse. The fuse F1, the pyroswitch P1 and the electronic triggering system are depicted. During its lifetime, the entire device is closed and the nominal current is flowing. The P1 resistance (copper bar) is lower than the F1 resistance. For instance, with a 400A pyroswitch, the on-state resistance is around 200µΩ and the resistance of a fuse is around 1-2 mΩ. Thus most of the nominal current (80% - 90%) flows through P1. Cycling performance and lifetime are improved in comparison to a simple fuse. Moreover, with the very low resistance of the entire system (~200µΩ), the on-state losses drastically decrease. Fuse F1 could be sized with a low nominal current caliber (10 – 20 % of I_N) and thus a low cost.

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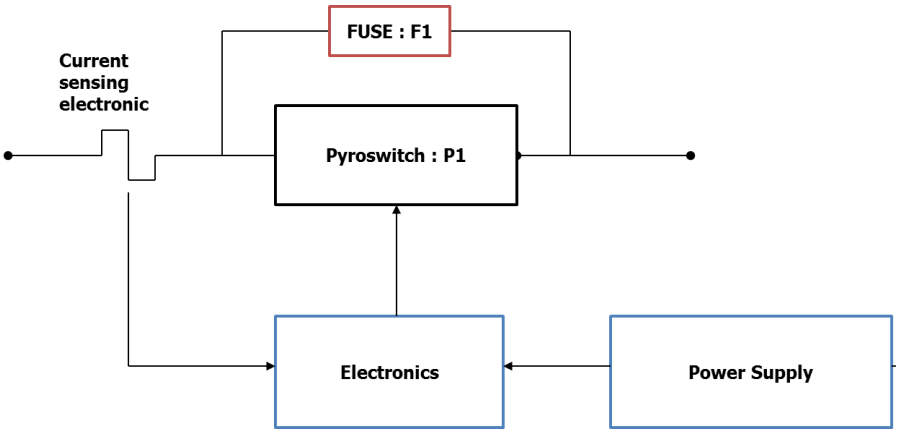

Fig. 5: Electrical Schematics of the Pyrofuse

Let's focus on the cut off. When the current abnormally increases because of a failure in the DC application, a sensor (Hall Effect or shunt) detects the fault current and sends the triggered signal to P1 thanks to a control board. As seen before, pyroswitch systems suffer from a risk of harmful arcing when cutting off a high voltage load. But in this case, a fuse F1 is situated in parallel and is still closed. Thus P1 cuts the copper bar without any voltage and the fault current flows through F1. As this fuse is underrated, it opens the circuit with a very short cut-off time (less than 300 µs). To summarize, the fuse is sized for the nominal voltage and underrated for the current. This new protection makes it possible to cut off high voltage (until 1500V) and high current (400-800A).

Comparison between pyro and conventional fuse

Whereas AC applications keep on growing at a moderate rate, MERSEN has encountered a booming demand in DC protection, dealing with fast emerging markets such as EV/HEV, battery storage, data-center, PV, traction or **electric aircraft**. To answer this, Mersen has developed a complete range of DC OCP devices. Among them, we can find fuses and pyrofuses and this section presents the comparison between the two technologies.

First let's focus on the advantages for each solution. Today DC fuses are ultra-fast acting fuses for large fault currents with a cost effective and a proven technology. A pyrofuse is a fast acting protection with a low cost technology. The conduction losses are close to zero and the system operates for small or large fault currents (fully configurable). Table 2 summarizes the performances of the different technologies. Both products are not resettable because they are used as an ultimate protection. The time to clear the fault is independent of the current for the pyrofuse and the time-current curve is totally tunable which is not the case for the fuse. The new solution has an excellent cycling performance with low conduction losses.

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Table II: Summary of the comparison between the pyrofuse and fuse

Family	DC fuse	Pyroswitch + fuse
Resettable	No	No
Time to clear high fault current	Excellent, 10 µS	Good, 1 ms
Time to clear low fault current	Slow to melt	Excellent
Cycling performance	Limited	Excellent
Conduction losses	80W (400A)	20W (400A)
Tunable Time-Current curve	Limited	Yes
Self-powered	Yes	Possible
Average market price	Low	Low

The new OCP has many benefits but the main problem is the electronic command. Indeed, this solution is not self-powered as a fuse and current sensor and electronic have to be added. In some applications, it is impossible to put this electronic in the required volume. For these reasons, a self-triggered pyrofuse has been developed. The next section will present the principle and the characterization of the ultimate protection.

Ultimate Protection

Principle

As seen before, pyrofuse protection shows excellent performances (cut-off time, volume, weight and cost). Unfortunately, in some applications, the current control command is not straightforward. Moreover, some protections need to be self-triggered to ensure ultimate protection of the electrical installation. All these reasons have led us to develop the self-triggered pyrofuse.

Figure 6 depicts the patented self-triggered pyrofuse (a) in nominal conditions and (b) with a fault current. Let's focus on the nominal conditions. The schematic shows the same pyrofuse in green, with pyroswitch PS1 and the parallel fuse F1. PS1 is split in two paths: the ignition one depicted by a resistor and the power one where the nominal current flows inside. In the previous section, the user had to add a control electronic to trigger the system. In this solution, the principle is to add a fuse (F2) in series which is designed for the nominal current but not for the nominal voltage. This fuse is used as current sensor and power generator for the pyroswitch trigger. In nominal conditions, current flows though F2 and PS1. If a fault current appears (figure 6 (b)), an electrical arc arises between the terminals of fuse F2. At this moment, nothing can stop the arc because F2 is not designed for the nominal voltage. This arc will be used as a voltage source by the

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initiator. R1 defines the current flowing in the ignition of PS1 and controls the opening speed of PS1. After the ignition, the principle is similar to a conventional pyrofuse described in the previous section. When the pyrofuse opens the circuit, the arc in F2 disappears and the entire system protects the application without external electronic.

The advantage of this system is that it is self-powered, similar to a conventional fuse. As F2 is not designed for the nominal voltage, the fuse has a small size and low watt losses. Thus the total losses are still lower than a conventional fuse.

The drawback is the lack of selectivity in the time current curve that we could have with the electronic control command. However, with a low voltage fuse, the selectivity is more easily tunable. The next section presents the test results.

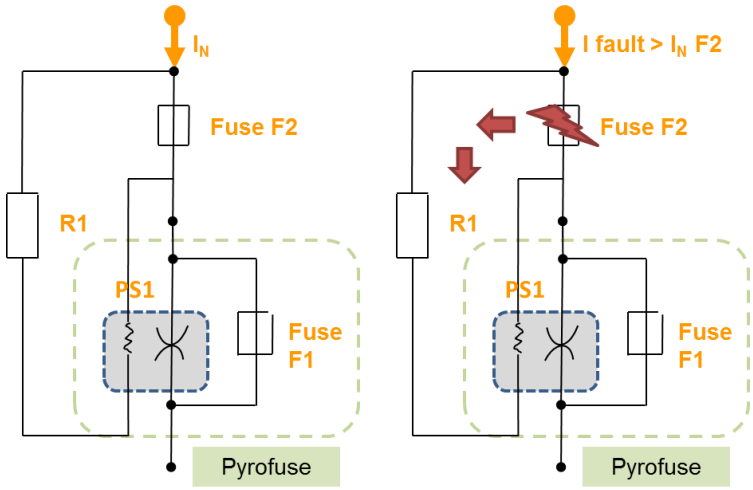

Figure 6: Schematic of the self-triggered pyrofuse in (a) nominal conditions and with (b) a fault current

Test **results**

In order to validate the self-triggered pyrofuse principle, several tests have been done in our labs. It has been tested under 500VDC with 11 kA fault current and the results will be presented in figure 7. The current is depicted in blue and the voltage in red. It is possible to share the wave form in 4 steps. Step 1 is the beginning of the short-circuit with the increase of the current through fuse F2 and PS1. When the current reaches a certain value, an arc appears in F2 (step 2) which increases the voltage and limits the current. During this step the energy of the arc is conveyed to the pyroswitch. In step 3, PS1 is triggered and the current flows in F1. This fuse melts, causing an overvoltage and a drop in current. At this moment the arc in F2 has not enough energy to be maintained. In step 4 the system has protected this application with a voltage of 500V and no current.

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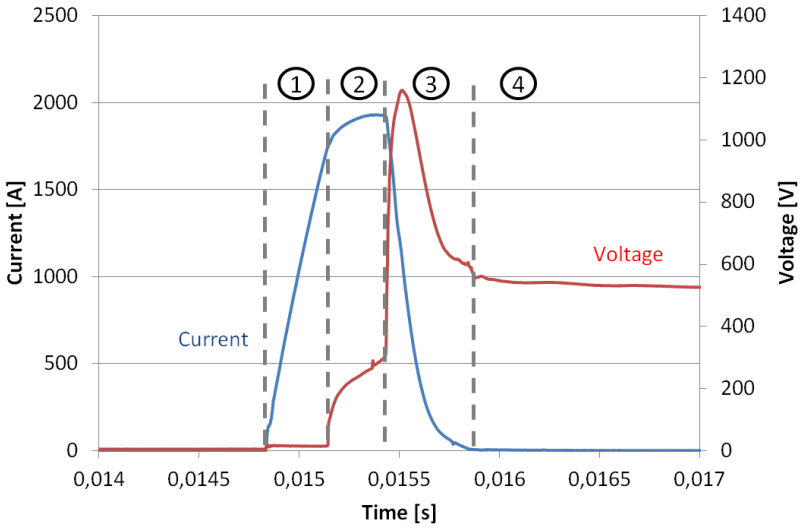

Figure 7: Waveforms of the current and the voltage during the switch-off

The advantage of the system is the limitation of the fault current which never reaches the maximum value. Moreover, this solution is completely autonomous.

Figure 8: Self-triggered pyrofuse – XpST

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Figure 8 presents the self-triggered pyrofuse we have developed at MERSEN. The entire system has a height of only 70 mm, a length of 135 mm and a width of 65 mm.

For aircraft application, the pyrofuse and the self-triggered pyrofuse have many advantages:

- Respond to DC transportation requirements.
- Excellent time to clear the high and fault current.
- Excellent cycling performance: load profiles in aircraft applications are becoming more complex. The cycling performance for the pyrofuse is independent of the load profile which simply the design.
- Very low conduction losses.
- Low average market price.

Conclusion

This delivrable presents the Fuse gen II overcurrent protection device for DC applications. The conduction path made by the pyroswitch and the clearing path made by a fuse bring the best of the 2 products, i.e. low voltage drop, high inrush current capability, high cycling performance, fast cutting of the busbar. Moreover the fuse presents an excellent capacity to clear high DC current. Tailored to the final application, these 2 devices bring the best performances for the More Electrical Aircraft.

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3.2 WP2. Semiconductor fuse design and fabrication

3.2.1 Task 2.1 Analysis of specification

The starting specifications have been extensively analyzed and fully identified by the partners and the customer. A specifications document have been generated and used for the analysis and developments works.

The next step was to compare the final specifications with the performances of existing SiC current limiter developed by the project partners, published in the literature or patented in previous related works. From this initial analysis, we have seen that some significant changes in the design approach and in the device technology were necessary to reach the targeted specifications. Concretely, the main challenges are related with the following specs:

- Low specific on resistance of the JFET to pass 80A with a voltage drop lower than 1V
- Adjust the technological and geometrical parameters to fit
    - Short-circuit and overload times
    - Current limiting capability (1ms at 600V)
    - Breakdown voltage higher than 900V
- Reduced size factor for the JFET SSCB (10cm x 10cm x 10cm), including positive and negative branch of the bus.

We are aiming a 10mOhm.cm2 current limiting JFET with 1 ms short-circuit capability.

This task has been performed successfully and no deviations were observed.

3.2.2 Task 2.2 Geometry design and optimization of the current limiter

D2.1 Report on SiC current limiter fuse design and mask set

In this task, 2D simulation work with numerical simulator has been performed by INSA Lyon in order to adjust the device basic cell geometry of the device to the specs. The modeling was performed using Sentaurus software. Electro thermal simulations during short-circuit operation have been performed, targeting 600V/1ms. An ideal channel thickness between 0.7um and 0.9um for a Ron around 6mOhm.cm2 is expected, as inferred from Figure 4.

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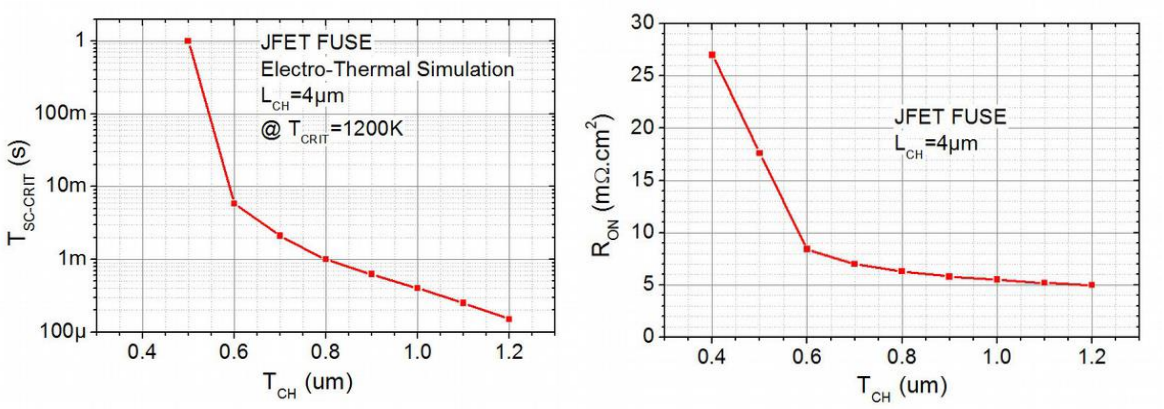

Figure 4. Channel thickness TCH optimization by means of finite elements simulations for the short circuit characteristics (left) and for specific on resistance Ron (right).

The final structure designed and optimized is drawn in Figure 5.

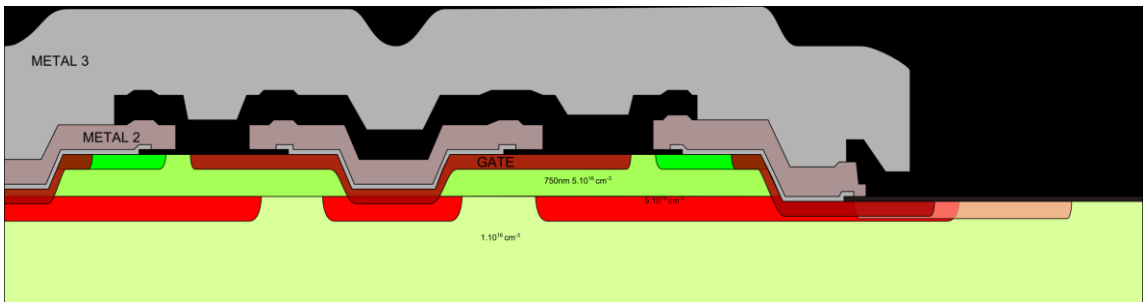

Figure 5. Cross section of the final structure of the current limiting JFET

A mask set including main limiter transistor and several test structures with designs variation have been drawn and integrated (see Figure 6)

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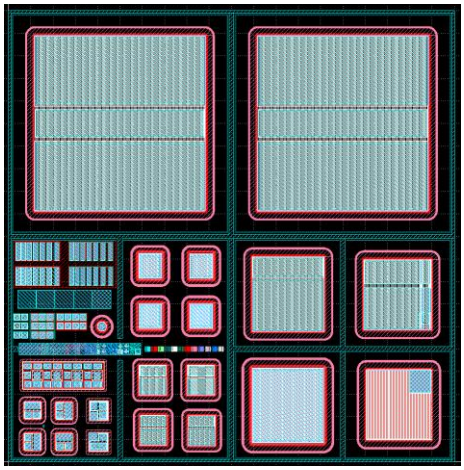

Figure 6. Fabrication Mask Set elementary field.

This task was performed successfully and no deviations were observed.

3.2.3 Task 2.3 Technology optimization and device fabrication

In parallel with the design and modelling task (Task 2.2), a first technology process has been discussed and defined. Several significant changes have been considered to simplify the fabrication accuracy. We added an Aluminum implantation step for form a P+ layer for gate contacts. It allows to remove one very critical etching step (with the need of very precise depth control) which shown in previous work to strongly affect the yield and performances of the fabricated structures. To increase the integration density, we also have considered a three metal level technology instead of two metal level used in previous works.

As a consequence, the technology is based on 10 photolithographic steps:

1. ALIGN: Alignment layer (photoresist as RIE mask)
2. PWELL: P+ implantation areas to create Pwell
3. NPLUS: N+ source layer implantation
4. ETCH: MESA etching to remove N-type channel epilayer down-to P-type buried layer over the active and termination area
5. PPLUS: 200-500nm P+ implantation to connect PWELL, create a field stopper and the gate of the JFET
6. JTE: termination implantation
7. CONT: Thin oxide layer opening (source & gate) and contact metallization (Ni, lift-off)
8. GATE-METAL: 500nm metallic layer to route the gate under the ILD
9. MET2: Thick final metal patterning

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10. PASS: Polyimide patterning, opening on bonding areas

Some preliminary processing tests have been performed in order to adjust etching profiles required by the new structure design. Concretely, we have explored new recipe for SiC dry etching in order to reduce the etching rate for a better control of the etched depth. A second objective of these tests was to increase the slope of the trench sidewall. This is necessary to optimize the buried gate connection in the new design considered in Task 2.2. A picture of former etching pillar and new technology pillars is shown in Figure 7.

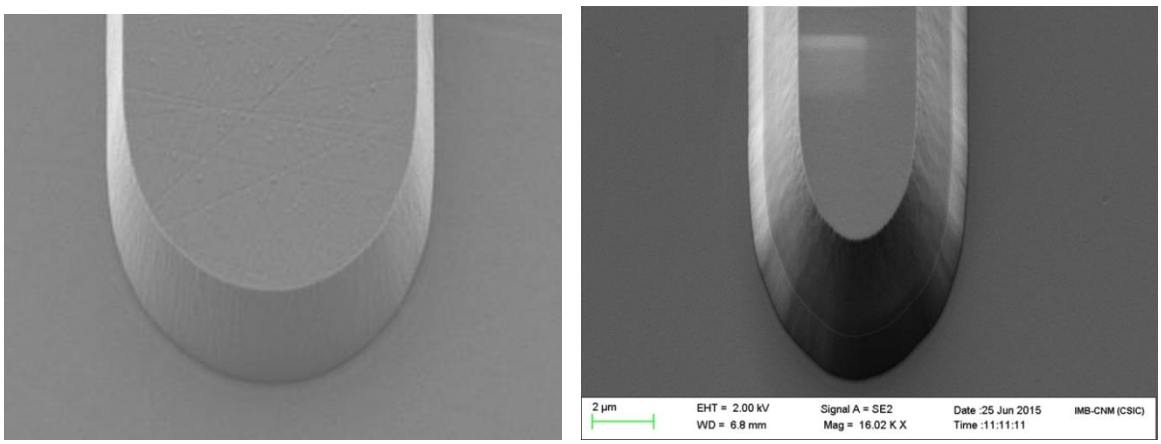

Figure 7: SEM pictures of a deep etched pillar with high aspect ratio (former technology) and new process pillar with increased sidewall slope and lower etch rate (new technology).

Once the photolithography mask set available from task 2.2, we have started the 1st batch of device fabrication in the CNM-CSIC clean room. Starting wafers with epilayers in the range of 12-14µm thick and 5e15 doped were purchased from different manufacturers. These epilayers are intended to provide 1.2kV voltage capability devices.

This task is running successfully with no deviations at this stage.

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3.2.4 Task 2.4 On-wafer characterisation of the current limiter

3.2.5 Task 2.5 Devices packaging

D2.2 SiC current limiter prototypes delivery

Design

The SiC Current limiter design has been reported in deliverable D2.1. Both the fabrication process and fabrication mask have been defined to match the electrical performances required for the fabrication of the SSBC prototype.

– Specifications:

- Blocking voltage > 540V
- Specific on resistance: 6 mOhm.cm^2
- Threshold voltage: V_{TH} = -12V

Fabrication Mask elementary field (left) and whole mask (right).

The goal is to design and fabricated SiC current limiter devices that will allow testing the new design against the bill of requirement.

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Fabrication Run

Several wafers have been processed in the CNM clean room. The reference of the process is run 8528-CLE. The mask set used is the CNM-SIC038. The following table resumes the wafer parameters and fabrication status.

Wafer reference	Parameters (Wepi/Nepi)	Targeted V_{br}	Status
W1- HB0730-25	Substrate N+	0V	Test wafers only for technology process development
W2- BQ1727-08	CREE wafer	1200V	Measured in INSA; with polyamide
W3- BQ1727-14	CREE wafer	1200V	Broken but one part is usable; Measured in INSA
W4- HB0730-09	CREE wafer	1200V	Wafer stopped after JTE implantation and high temperature annealing
W5- R019-14	Norstel wafer	1200V	Measured in INSA; with polyamide

The process consists of 12 photolithographic mask levels and a total of 97 process steps. After the second photolithographic step and associated implantation process, an epilayer re-growth step is necessary to define the channel. This step is critical in the sense that the thickness and doping of this epilayer will define the JFET characteristics. A difference in the thickness with the targeted value may strongly affect the posterior etching process made to reach the buried implantation of the gate.

A novelty included in this process is the triple metal levels. This is necessary to increase the integration density and to simply the device 3D design and structure. It should then allow a higher current limiting capability.

In the next table, a list of the main technology steps together with its impact and novelty is presented.

1. Alignement marks photolithography etching	No critical dimensions
2. Burried P-gate implantation photolitography	Critical dimension
3. Epilayer re-growth	Thickness and doping highly critical
4. N+ source implantation photolitography	No critical dimensions
5. Gate etching step photolithography and etching	Etching depth highly critical and depends on step 3
6. P+ gate implantation photolitography	Concerns with implantation on the etched

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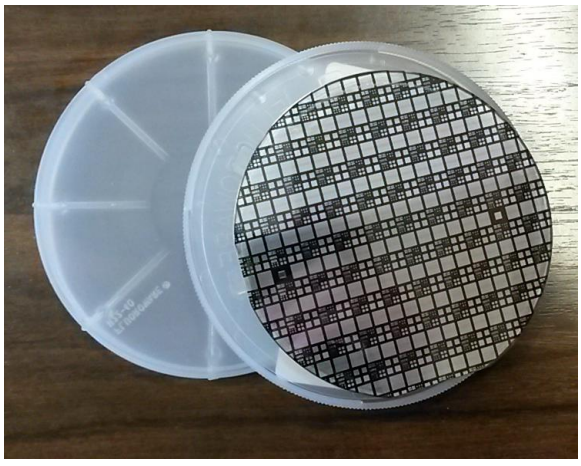
	slope
7. JTE implantation photolitography	No critical dimensions
8. High temperature annealing	Very standard process at CNM; no issues
9. Field oxide photolithography and etching (contact opening)	Critical dimensions
10. Contact metal photolithography and etching	Standard process at CNM
11. High temperature metal stack photolithography and etching	New step in the technology
12. Interlevel oxide deposition, photolithography and vias etching	New step in the technology; critical etching step
13. Thick metal deposition, photolithography and etching	New step in the technology but not critical
14. Polyamide deposition, photolithography and etching	Issues with polyamide adherence

Pictures of 4'' fabricated wafer.



Conclusion

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Even if the processed devices are operating, these samples are too resistive in forward mode for the SSCB prototype. The devices are almost all normally off or have a very low threshold voltage (-1V), which would be good if the on-resistance would not be so high.

FIELD	DEVICE	V_{TH} I_{DS}<100nA, V_{DS}=0.1V	I_{D-on} V_{DS}=0.1V, V_{GS}=0V	I_{D-off} V_{GS}= -3V, V_{DS}=50V
X5Y5 	JFET1	- 0.6 V	18 µA	50 nA
	JFET2	- 0.7 V	39 µA	9 nA
	JFET3	- 0.55 V	723 uA	15 nA
	JFET4	- 0.78 V	488 uA	0.05 nA
	JFET5	- 0.7 V	351 uA	0.70 nA
X8Y5	JFET1	+ 0.2 V	60 nA	150 nA
	JFET2	0 V	89 nA	350 nA
	JFET3	0.2 V	- 10 nA	360 nA
	JFET4	-0.05 V	500 uA	500 nA
	JFET5	0 V	100 nA	500 nA

The observed behavior is due to a thinner channel thickness that targeted. The effective channel thickness has been estimated to (~500nm). This can be caused by either an epi-layer parameter deviation or to fabrication process variations.

Correction actions taken

Some physical analysis have been performed (SIMS, FIB) and several validation done with the epitaxy provider.
SIMS analysis allowed certifying the delivered epilayer are in accordance with the specified parameters. Then, various options are possible to optimize the device fabrication process:

- To Increase of epitaxial layer thickness and tuning the doping value
- To modify the P+ implantation parameters to better control the final channel thickness
- To modify some of the process steps parameters in order to reduce the gate leakage current

A new fabrication batch has been launched in order to correct the processing parameters and reach the targeted specs for the devices.

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3.3 WP3. Module characterization and validation

3.3.1 Task 3.1 Fuse module standalone testing

MS3 Start fuses I testing

The following table (Table 2) summarizes the simulations and the results of the fuses prototype gen I, whose specifications are:

- 830A <10ms
- 11kA <320us

		13260- 4 rows	13260- 3 rows	19449- 4 rows	19449- 3 rows
250A	Tpa	Simulation:10.9s	Simulation:10.8s	Simulation:6.57s	Simulation:6.22s
		Test: still close	Test: still close	Test: still close	Test: still close
<3s	Total Time	Simulation:10.92s	Simulation:10.9s	Simulation:6.59s	Simulation:6.24s
		Test:	Test:27.8ms	Test:13.28ms	Test:14ms
	Uarc	Simulation:558V	Simulation:554V	Simulation:560V	Simulation:551V
		Test:	Test:	Test:	Test:
	Iarc	Simulation:251A	Simulation:251A	Simulation:250A	Simulation:251A
		Test:	Test:	Test:	Test:
830A	Tpa	Simulation:16.7ms	Simulation:16ms	Simulation:6.8ms	Simulation:6.8ms
		Test:25ms	Test:23ms	Test:7.7ms	Test:7.7ms
<10ms	Total Time	Simulation:25ms	Simulation:32ms	Simulation:13.8ms	Simulation:21.5ms
		Test:28ms	Test:27.8ms	Test:13.28ms	Test:14ms
	Uarc	Simulation:614V	Simulation:559V	Simulation:674V	Simulation:557V
		Test:949V	Test:825V	Test:866V	Test:809V
	Iarc	Simulation:822A	Simulation:823A	Simulation:745A	Simulation:745A
		Test:827A	Test:843A	Test:745A	Test:747A
11kA	Tpa	Simulation:698us	Simulation:698us	Simulation:614us	Simulation:613us
		Test:523us	Test:529us	Test:455us	Test:452us
<320us	Total Time	Simulation:4.8ms	Simulation:5.4ms	Simulation:4.6ms	Simulation:5.5ms
		Test:3.5ms	Test:3.5ms	Test:3.44ms	Test:3.67ms
	Uarc	Simulation:777V	Simulation:700V	Simulation:876V	Simulation:710V
		Test:708V	Test:655V	Test:831V	Test:717V
	Iarc	Simulation:2200A	Simulation:2200A	Simulation:1950A	Simulation:1950A
		Test:2573A	Test:2570A	Test:2287A	Test:2278A

Table 2. Comparison of the prototypes made by MERSEN

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The tests show good results compared by simulation. The first fuse generation does not allow shaping the time to current curve. Improvement will be done on the second fuse generation by using silver or bi-metal element, ceramic body and as filler sand to quench the energy during clearing.

Conclusion

Our experience in the fuse element design allows us to shape the time current curve in order to meet certain gates. This deliverable presents the work done to design a fuse element and test it. The reduce section area allows us to test the new design against the bill of requirement. Simulation has been used to verify the fuse design. After test analysis of the first fuses batch, a redesign will be considered for the second production batch.

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3.3.2 Task 3.2 SiC current limiter hybrid module testing

D3.2 Report on SiC current limiter tests results and analysis

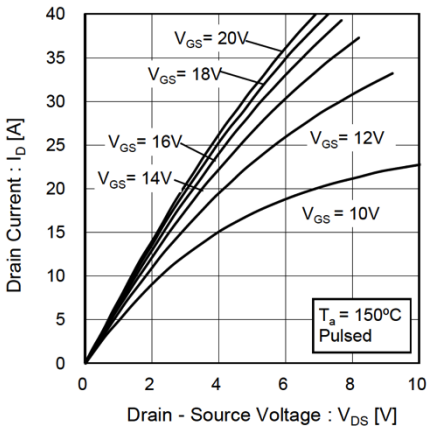
SiC Current limiter module design.

SiC current limiters issues from the project are not matching the electrical performances. Elementary dies are too resistive and current level is tow low. An alternative solution has been implemented. We have replaced the SiC current limiter devices by 16 SiC MOSFET. Doing so, we have been able to validate:

- Both the modules and the PCB design, fabrication and assembly,
- The functionalities of the SiC current limiter,

Several SiC MOSFETs have been characterized in operating modes corresponding to the application (short-circuit, nominal). Among various providers (CREE, ROHM), we have selected 1.2kV 80mOhm – 40A SiC MOSFET from Rohm. Indeed as presented on Figure 1, the Rohm MOSFET are presenting the best trade-off in terms of electronics performances in steady state and short-circuit modes.

The maximal critical energy depending on bus voltage has been extracted, as well as the voltage drop depending on operating temperature. This value [$E_{SC-CRIT}$ = 0.4J] is input information for the design of the alternative module demonstrator.

<table>
<tr>
<td> 
</td>
<td>Electrical main features.

MOSFET on-resistance:
- 110mOhm @ at 150°C,
- 80mOhm @ room temperature.
DC current = 40A
Pulsed current (10 us) = 80A.
$E_{SC-CRIT}$ = 0.4J
Breakdown voltage = 1.2 kV</td>
</tr>
<tr>
<td>SiC devices typical output characteristics (Ta = 150°C)</td>
<td></td>
</tr>
</table>

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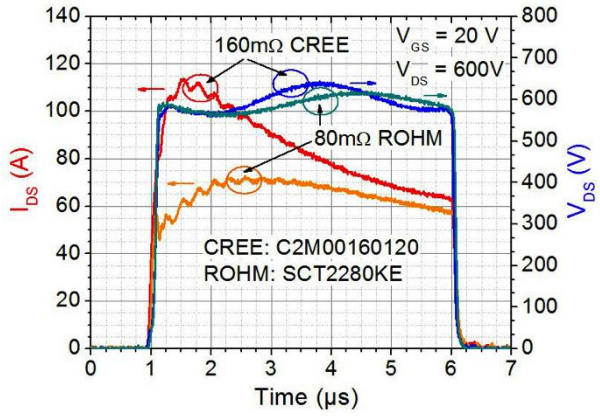
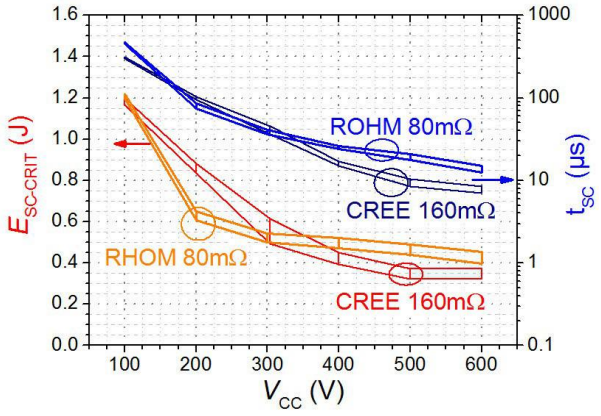


Short-circuit waveform at 600V on 80mΩ ROHM and 160mΩ CREE VMOS.



Critical energy and length of SC depending on bus voltage (V_{CC}) up to 600V for CREE and ROHM 1200V SiC-MOSFETs.

Figure 1. SiC power MOSFET characterization in short-circuit mode.

The Table 1 resumes the design choice of the module considering the electrical constrains. In order to keep the voltage drop below 250mV at 83 A (for 2 phases), the on resistance of each phase must be lower than 1.5 mOhm. At a temperature of 150°C, 73 devices connected in parallel are needed to match the voltage drop constrains. Considering an operating mode limited between 80°C and 125°C only 64 devices in parallel would be required.

Table 1. Sub-module design considerations.

	Unit	Value	Time	Module state	Impact on design (Ta = 80°C)
Voltage drop (@ 83A)	mV	< 250	DC	Sustain	Device number = 64
Surge 1	A	120 A	60s	Sustain	Elementary die current = 1.8 A (Only 3 dies are required for 120A)
Surge 2	A	250 A	3 min	Sustain or open	Elementary die current = 3.9A (Only 7 dies are required for 120A)
Short-circuit	A	700 A	< 350 us	Sustain or open	E_{SC-MAX} = 0.4J -> circuit must be opened in less than 60us.
Lightning	A	< 700A	< 310 us	Let pass or open	

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Characterization of prototypes

A specific test bench has been designed and fabricated in order to test modules in dynamic mode. The setup is composed of several functional boards:

- Control boards (micro-controller and CPLD), implementing a control state machine enabling solid-state switch to operate in safe condition (i(t) tripping curve by software control).
- Master switch (composed of 10 silicon BIMOSFET connected in parallel)
- Specific drivers
- Optical link between modules
- R,L load and DC-BUS capacitor.
- Current limiter sub-module
    - Discrete version of module, composed of TO247 SiC MOSFET in parallel (2x 10 device)
    - Project power module, composed of SiC MOSFET in parallel (2 x 8 devices)

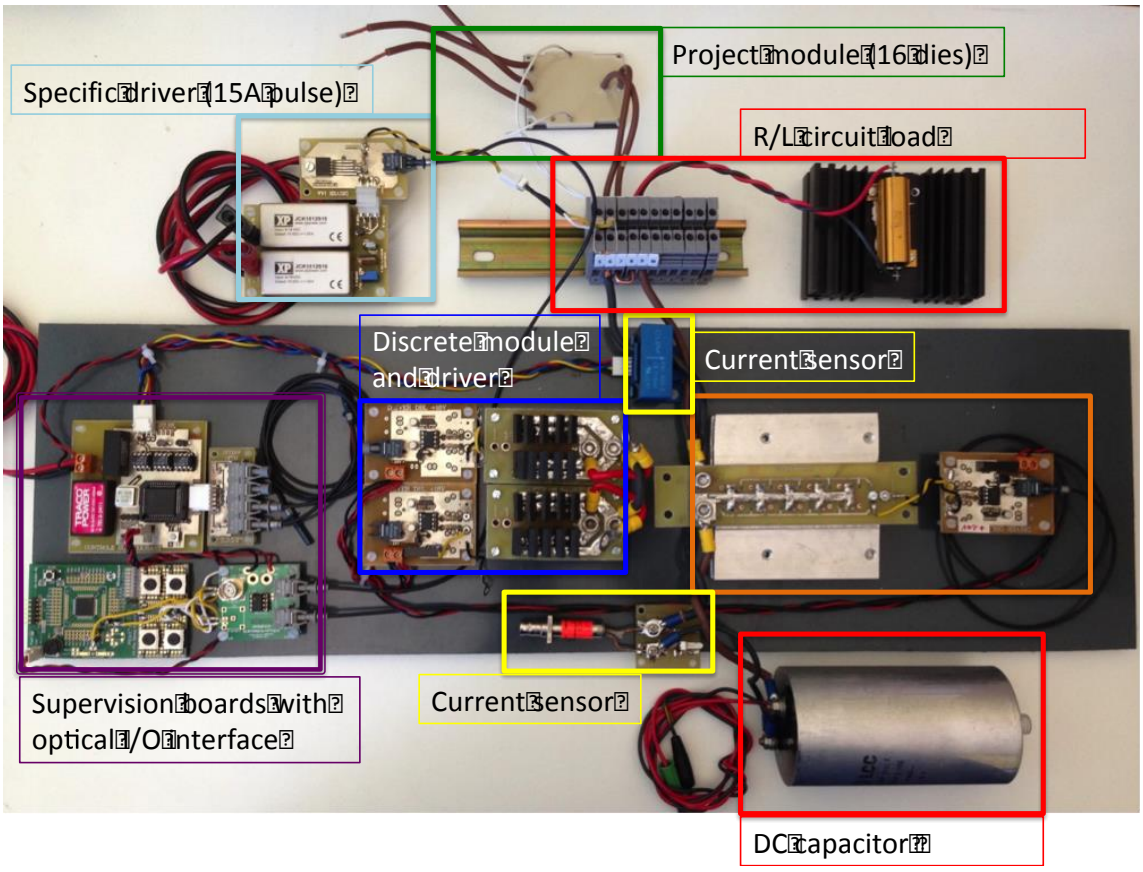

Figure 2. Picture view of the experimental test bench.

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Functional blocs. State machine control board (violet) ; Master switch board (orange); Discrete and integrated SiC Current limiter boards (green/ blue); Current sensing element (yellow): LEM (HAL-400S) , resistive shunt.

This setup allows characterization up to 1kV with current capability up to 1.5kA in pulsed mode. Fast switching and repetitive pulses are possible, with a repetition period of 300ms (limitation due to the high voltage power supply capability).

Conclusion

Even if the processed SiC current limiting devices fabricated in WP2 are operating, the samples are too resistive in forward mode for the SSCB prototype. The devices are almost all normally off or have a very low threshold voltage (-1V), which would be good if the on-resistance would not be so high.

An alternative solution has been chosen for the fabrication and the characterization of the SiC current limiter: implement commercial SiC devices. One issue is the fabrication yield of power module. Indeed, using commercial devices implies to increase the number of die to connect in parallel. We end up with 3 functional modules for 5 modules fabricated.

The experimental measurements performed on delivered modules allows to validate:

- The control board able to drive 16 MOSFET connected in parallel
- The compatibility of the modules with the BOR (I(t) tripping curve (low on resistance, current sensing).

Full rated power characterization wasn't possible. Indeed the low number of functional modules don't makes possible to test modules at high current levels.

The module assembly process is quite challenging. The fabrication failure (3modules functional over 5) points out the necessity to reduce the straight inductances within the power module, as well as the number of SiC devices to parallel. Having SiC custom devices, we should be able to reduce the number of parallelized MOSFET, increasing thereby the fabrication yield of the sub-modules.

Performance analysis and perspectives.

To achieve a high level of reliability and performances for a SiC current limiter module, it would be necessary:

- To stabilize the SiC current limiter power device fabrication
- To reduce the fabrication delay of the boards,
- To reduce the number of parallelized devices.

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A new fabrication batch has been launched in order to correct the processing parameters and reach the targeted specs for the devices. Devices would be delivered after the end of the project. However, the preliminary measurements point out the possibility to address the Cleansky objective.

The cost estimation of such a solution will be higher than 5k€, assuming that SiC Die cost could be around 35€ /unit, and considering the high cost of a custom packaging.

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3.3.3 Task 3.3 Final optimal module testing

D3.3 Report on engineering tests on final fuse module

Samples have been tested under 500VDC with different faults current and the results are presented in the following table:

		Fuse solution	**Hybrid solution**
250A <3s	Clearing time	Still closed	540 ms
830A <10ms	Clearing time	6.8 ms	6 ms
11kA <320us	Clearing time	698 us	300 us
Aging 120 A >10 000 cycles	Cycles	2800 cycles	>20 000 cycles

Figure 7 presents the 11kA fault current. The current is depicted in blue and the voltage in red. It is possible to share the wave form in 4 steps. Step 1 is the beginning of the short-circuit with the increase of the current through fuse F2 and PS1. When the current reaches a certain value, an arc appears in F2 (step 2) which increases the voltage and limits the current. During this step the energy of the arc is conveyed to the pyroswitch. In step 3, PS1 is triggered and the current flows in F1. This fuse melts, causing an overvoltage and a drop in current. At this moment the arc in F2 has not enough energy to be maintained. In step 4 the system has protected this application with a voltage of 500V and no current.

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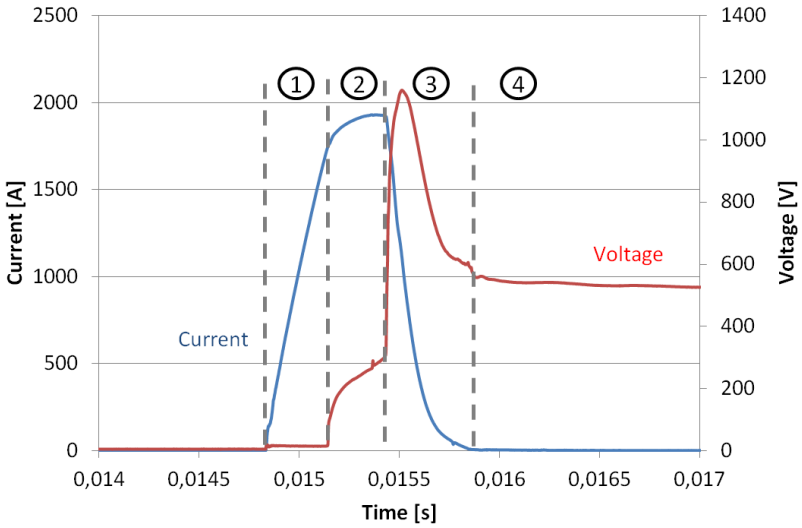

Figure 7: Waveforms of the current and the voltage during the switch-off

The advantage of the system is the limitation of the fault current which never reaches the maximum value. Moreover, this solution is completely autonomous.

Prototype

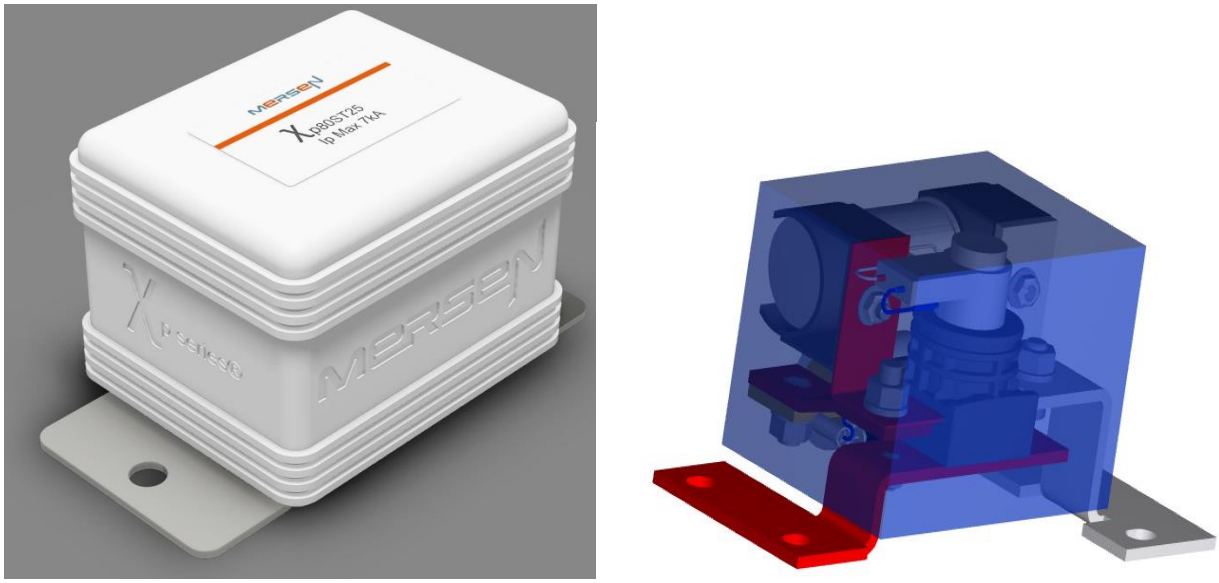

Figure 8: Self-triggered pyrofuse – XpST

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Figure 8 presents the self-triggered pyrofuse we have developed at MERSEN. The entire system has a height of only 70 mm, a length of 135 mm and a width of 65 mm.

For aircraft application, the pyrofuse and the self-triggered pyrofuse have many advantages:

- Respond to DC transportation requirements.
- Excellent time to clear the high and fault current.
- Excellent cycling performance: load profiles in aircraft applications are becoming more complex. The cycling performance for the pyrofuse is independent of the load profile which simply the design.
- Very low conduction losses.
- Low average market price.

Conclusion

This delivrable presents the final module overcurrent protection device for DC applications. The conduction path made by the pyroswitch and the clearing path made by a fuse bring the best of the 2 products, i.e. low voltage drop, high inrush current capability, high cycling performance, fast cutting of the busbar. Moreover the fuse presents an excellent capacity to clear high DC current. Tailored to the final application, the final device bring the best performances for the More Electrical Aircraft.

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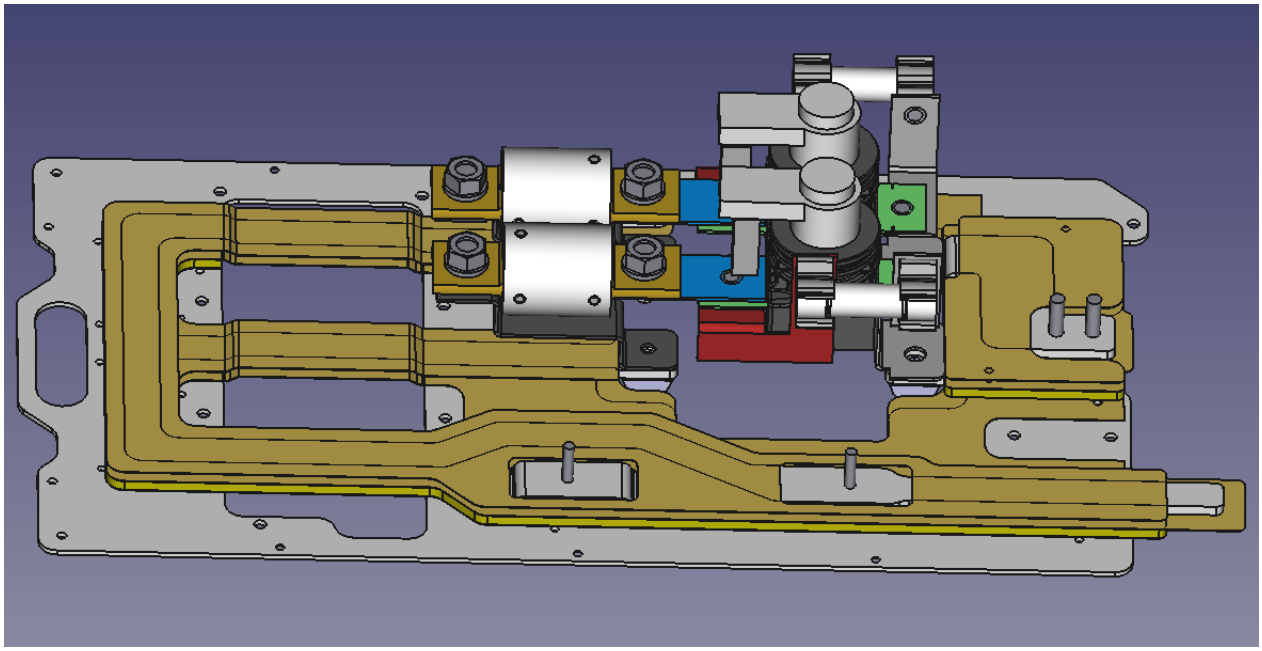
3.3.4 Task 3.4 TRL validation and support to integration in EPDS demonstrator

D3.4 Final optimal prototype delivery

Prototype

This paper presents a novel solution based on a hybridization of fuses and pyroswitch components that may answer new DC protection needs.



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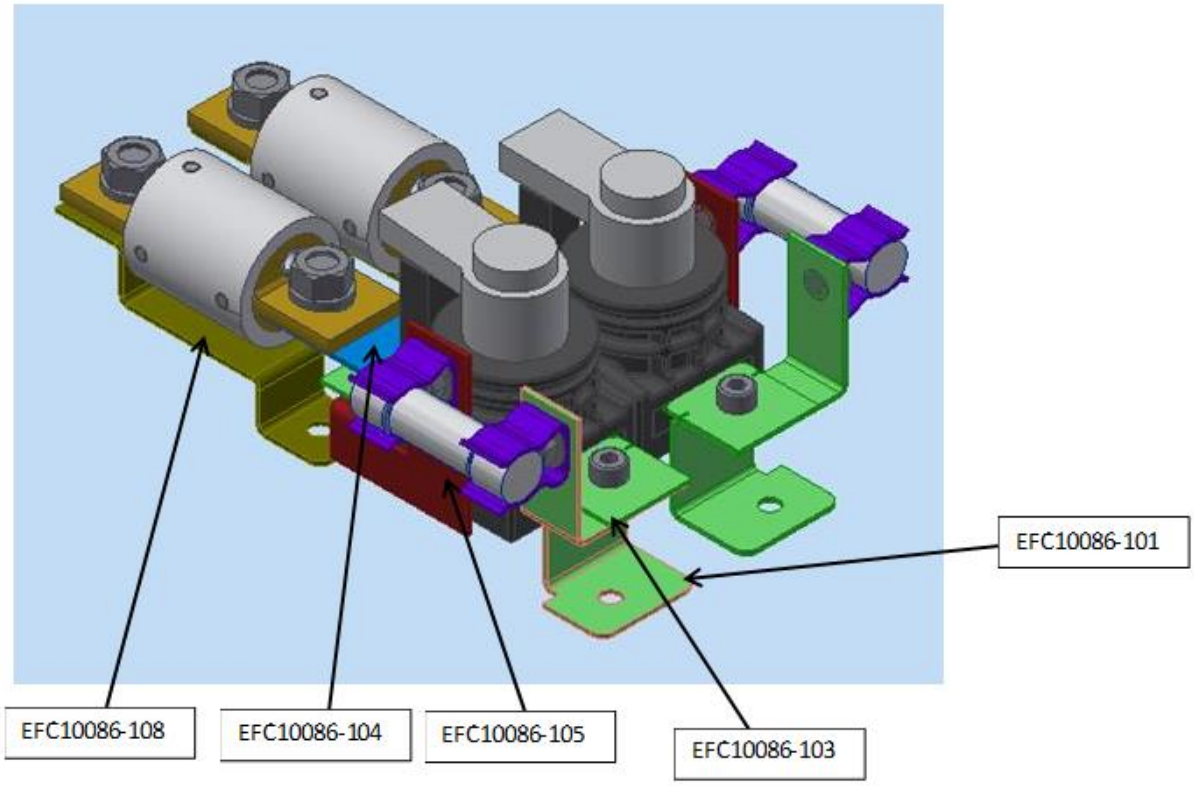
Clean

Sky



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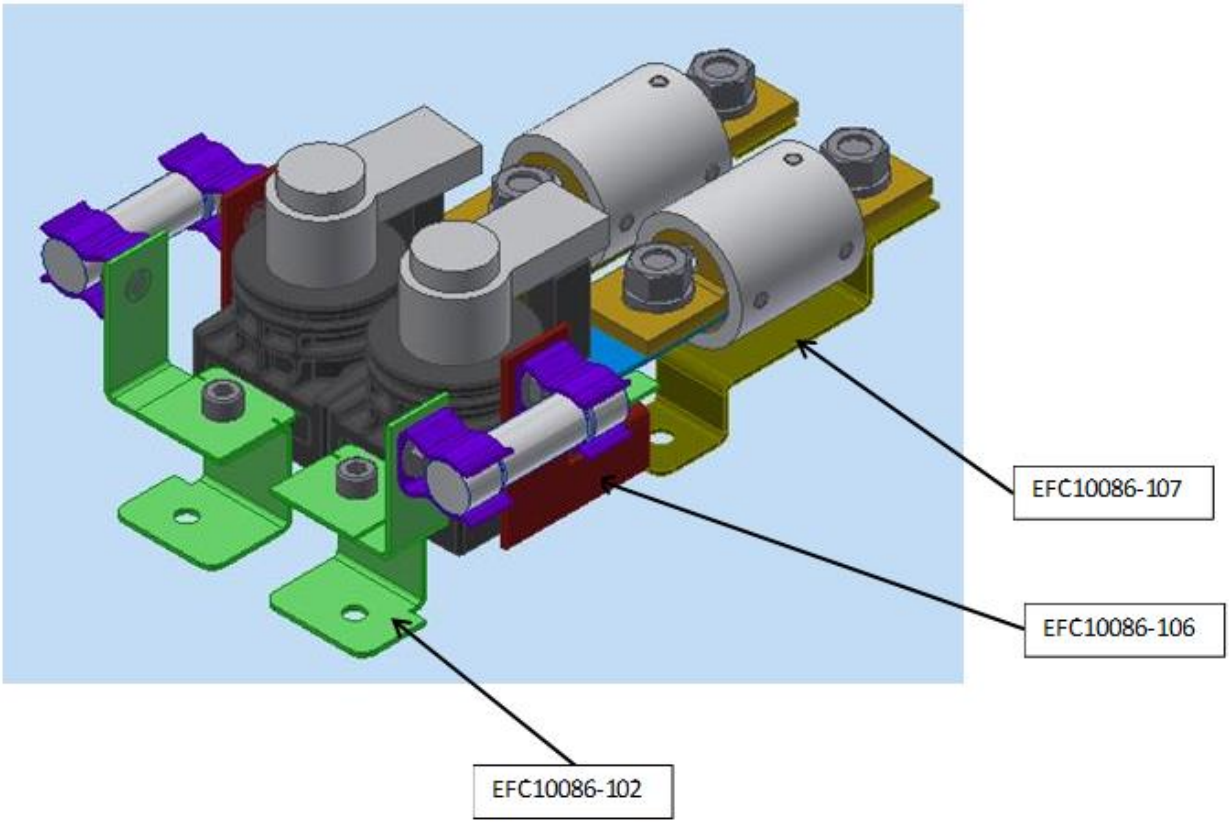

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4. Description of the potential impact

4.1 Technical objectives

Simulation has been used to verify the fuse design. After test analysis of the first fuses batch, a redesign has been considered for the second production batch. The second batch is an hybrid solution based on fuse and pyroswitch technologies. The conduction path made by the pyroswitch and the clearing path made by a fuse bring the best of the 2 products, i.e. low voltage drop, high inrush current capability, high cycling performance, fast cutting of the busbar. Moreover the fuse presents an excellent capacity to clear high DC current. Tailored to the final application, the final device brings the best performances for the More Electrical Aircraft. We have launched the building of 200 devices to qualify the DO160. Today the situation is at follow: the ‘‘hybrid fuse” developed by Mersen fit the early protection/clearing requirement of the project. We were expecting to test our device at Airbus before engaging any DO160 certification/testing. Our prototypes are ready for this test but the testing at airbus has been delayed to unknown date. More urgent testing at Airbus have taken priority. Mersen have made the decision not to engage any DO160 testing/certification before the testing at Airbus. No need to do DO160 if we fail the testing at Airbus, it would have been spending money too early. Current situation is complicated since we don’t know when the testing at Airbus will occur and we need to close the project. Since we cannot any longer keep the project open Mersen proposed to close it without DO160 standard Eng. Tests. Nevertheless, since samples are ready to test, Mersen will perform the testing at Airbus once their lab becomes available. Of course Mersen will not seek any EU funding for this deliverable/task not completed. Mersen estimates at 3pm the load that would has been used to carry on D0160 Eng. testing.

Concerning the SiC demonstrator, even if the processed SiC current limiting devices fabricated in WP2 are operating, the samples are too resistive in forward mode for the SSCB prototype. The devices are almost all normally off or have a very low threshold voltage (-1V), which would be good if the on-resistance would not be so high.

An alternative solution has been chosen for the fabrication and the characterization of the SiC current limiter: implement commercial SiC devices. One issue is the fabrication yield of power module. Indeed, using commercial devices implies to increase the number of die to connect in parallel. We end up with 3 functional modules for 5 modules fabricated.

The experimental measurements performed on delivered modules allows to validate:

- The control board able to drive 16 MOSFET connected in parallel
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Full rated power characterization wasn’t possible. Indeed the low number of functional modules don’t makes possible to test modules at high current levels.

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The module assembly process is quite challenging. The fabrication failure (3modules functional over 5) points out the necessity to reduce the straight inductances within the power module, as well as the number of SiC devices to parallel. Having SiC custom devices, we should be able to reduce the number of parallelized MOSFET, increasing thereby the fabrication yield of the sub-modules.

To achieve a high level of reliability and performances for a SiC current limiter module, it would be necessary:

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- To reduce the fabrication delay of the boards,
- To reduce the number of parallelized devices.

A new fabrication batch has been launched in order to correct the processing parameters and reach the targeted specs for the devices. Devices would be delivered after the end of the project. However, the preliminary measurements point out the possibility to address the Cleansky objective.

The cost estimation of such a solution will be higher than 5k€, assuming that SiC Die cost could be around 35€ /unit, and considering the high cost of a custom packaging.

The cost estimation of the hybrid fuse solution is estimated as 300€, which is much lower but this device isn't ressetable.

4.2 Management objectives

The management organization comprises three levels: the global management, the administrative management of the project, and the management of WPs. The management system has been set up at the beginning of the project life and has been coordinated by Mersen that implemented and deployed the necessary management procedures (costs, people, facilities, communication, knowledge, legal aspects and IPR and risks). The management has been simple as there are only 3 partners, used to work together since many years.

The work package managers have been designed for each WP. The work package leader is involved in the detailed coordination, planning, monitoring and reporting of the work package and for the detailed communication with other work packages. More specifically, the work package leaders are responsible for:

- Leading the WP including technical and management activities, continuously monitoring the progress of the participant tasks, controlling its efficiency
- Reporting WP/task activity to the whole consortium in four-month reports

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- Ensuring that milestones and deliverables of the WPs are fulfilled, organizing, if needed, special meetings to determine suitable measures to be taken

4.3 Dissemination.

The results from this project will be used to expand partners´ product portfolio to include new fuses and limiting systems for aircraft application, considering specific package for altitude working conditions. This is clearly a market segment that will increase in importance over time. The challenge of introducing these new products to the global market will be easier and less risky as they have been specified, developed and tested in open co-operation with Clean Sky platform.

In addition, the results of this project may clearly have applications in other industrial fields. With the growth in DC renewable energy like PV linked with the need of energy storage for smart grid applications and DC energy distribution come the need of DC protection. This study will not only answer a particular application demand like aircraft DC distribution protection but also all future DC networks like, but not limited to, DC data center working at higher DC voltage, Capacitor bank for large to medium application for smart grid and private DC energy production. We can foresee the use of DC circuit protection in for example battery bank or supercapacitor bank. In traction applications full EV or hybrid HV and for large vehicles, trucks, trams, busses, shipboard… this device will answer and demand not yet or partially fulfil. Also smart DC protection will be needed, controllable protection from high fault current to low fault current will be a plus and will be attractive to all future DC distribution network. 1 to 1.5 MW batteries bank for smart grid application use standard DC breakers that not really fulfil the need of customers.

The early adopters of these hybrid fuses are clearly the EV car manufacturers. We have been testing this market with the hybrid fuse and we have strong demand for the performance is breaking to this field of applications. We are able now to cover application up to 1000 VDC, fault current up to 15 kA with a device rated up to 800 A RMS.

We foresee as well application in AC, where the fault current is too low to melt standard fuse. The hybrid fuse can be turned off with an external triggering signal. Top of it with the self-trigger function added to our design we foresee the utilization of this device as a backup device for standard breakers. For low fault current the breaker open the circuit, for high fault current our device will open the circuit. This approach will simplify the design of the breaker therefor the its cost.

As far as quantities the aircraft applications will represent only small quantities of devices versus the need in PV for example. We foresee the need of new DC current limiting device in PV sting, in PV sub array and main DC fuse. If we use the currently sold quantities in PV and/or EV applications we can foresee annual quantities in millions of pieces. Even though we could not finalize the testing with our SiC design we still believe that the SiC design will address a niche like current limiting/clamping for Li-Ion battery cell application. This will boost the use of SiC, therefore will beneficiate European SiC component manufacturer. This will certainly create a need to SiC European manufacturer i.e. creating high tech jobs. Same analysis can be done with new DC distribution network, same quantities but this is still a growing application.

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